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(54) Title of the invention: Data exchange device
(57) Abstract:
Purpose: To obtain a data exchange device which is capable of making a unit switch have a multistage constitution, expanding scale and simultaneously and efficiently handling multi-address data, and is capable of storing plural low speed interfaces and high speed interfaces.
Constitution: This device is composed of the multistage connection part P provided with plural of first unit switches S1 and second unit switches S2 having 8 input lines and 2 output lines. The first unit switches S1-1 to S1 to 4 and the second unit switches S2-1 are connected on the first stage and the second stage, respectively, in a line concentration shape, as shown on a drawing. Only the unit switches S1 are provided with tables T-1 to T-4 defining the plural output lines which should output multi-address data. Input ports #0 to #31 are inputted in multistage connection parts P-1 to P-16 by branching the input ports. Output ports are assigned two by two to the multistage connection part P and the outputs to output ports #0 to #31 can be performed by 16 multistage connection parts P-1 to P-16.

[Claims]

[Claim 1] A data exchange device which has a multistage connection part exchanging inputted copied multiple address data based on a predetermined rule defined preliminary, and outputting to an output port of the multiple address point eventually, including a plurality of input ports and a plurality of output ports, and between a plurality of input ports and a plurality of output ports, a plurality of unit switches which exchange data between a plurality of incoming lines and a plurality of outgoing lines are arranged to at least 2 steps, when data is exchanged between a plurality of input ports and a plurality of output ports and multiple address data is inputted, in a data exchange device outputted to a plurality of output ports which copied the mentioned above multiple address data and were appointed preliminary, making a unit switch of the 1st step into the 1st unit switch, and a unit switch after the 2nd step is made into the 2nd unit switch, if a plurality of 1st unit switches have necessity from a certain input port to inputted multiple address data, while exchanging for a multiple address copy of data and outputting a plurality of copied multiple address data to the outgoing line corresponding to an output port of the multiple address point, respectively, the 2nd unit switch inputs copied multiple address data which has a plurality of unit switches in the preceding paragraph, and is outputted to it from the outgoing line of a plurality of unit switches of the mentioned above preceding paragraph.

[Claim 2] The data exchange device according to claim 1 assigning an output port which branches and inputs into a plurality of the mentioned above multistage connection parts data into which the mentioned above multistage connection part was inputted in a plurality of preparations and an input port, is different in the mentioned above multistage connection part, respectively.

[Claim 3] The data exchange device according to claim 1 or 2 including a table where the above mentioned 1st unit switch defined plurality of outgoing lines which should output each

multiple address data, a multiple address processing means which judges the outgoing line which should output multiple address data by referring to the mentioned above table, and is exchanged for a multiple address copy of data.

[Claim 4] The data exchange device according to claim 1, 2 or 3 characterized by that the above mentioned 2nd unit switch determines the outgoing line which outputs copied multiple address data based on an incoming line number of incoming line which inputs copied multiple address data.

[Claim 5] The data exchange device according to claim 3 or 4 characterized by that the above mentioned 1st unit switch determines the outgoing line which should be carried out the multiple address from the mentioned above table based on both or one of two of a virtual path identifier of multiple address cells, and a virtual channel identifier, the mentioned above data exchange device is a cell exchange device for which a cell with a virtual path identifier and a virtual channel identifier in an Asynchronous Transfer Mode communication method (ATM communication method) is exchanged, the mentioned above table defines a plurality of outgoing lines which should output multiple address cells to both or one of two of a virtual path identifier and a virtual channel identifier.

[Claim 6] The data exchange device according to claim 3 characterized by that the mentioned above table is independently provided to each 1st unit switch, respectively.

[Claim 7] The data exchange device according to claim 3 characterized by that the mentioned above table is provided in common to a plurality of 1st unit switches.

[Claim 8] The data exchange device according to claim 3 or 4 characterized by that the mentioned above table defines the outgoing line which should output multiple address cells to a multiple address identifier and the above mentioned 1st unit switch determines the outgoing line which should be carried out the multiple address from the mentioned above table based on a multiple address identifier, the mentioned above data exchange

device is a cell exchange device for which a cell is exchanged, and a cell exchange device is provided with a multiple address identifier allocation means which assigns a multiple address identifier which identifies multiple address cells in the preceding paragraph of an input port to each multiple address cells.

[Claim 9] The data exchange device according to claim 8 characterized by that the mentioned above multiple address identifier allocation means is established to an incoming line group which includes a plurality of the mentioned above input ports, respectively.

[Claim 10] The data exchange device according to claim 1 outputting multiple address data corresponding to a plurality of the mentioned above low speed interfaces to an output port in which a plurality of the mentioned above low speed interfaces are accommodated, the mentioned above data exchange device is provided with an output port in which a plurality of low speed interfaces are accommodated, and the above mentioned 1st unit switch, exchange for a multiple address copy of data corresponding to a plurality of the mentioned above low speed interfaces, and the above mentioned 2nd unit switch.

[Claim 11] The data exchange device according to claim 10 including separation circuits which separate data outputted from the output port, and are outputted to the mentioned above low speed interface while the mentioned above data exchange device is connected to the latter part of one of the mentioned above output ports further at least and connecting a plurality of low speed interfaces, a timing generating means which generates identification timing for operating the mentioned above separation circuits, the above mentioned 1st unit switch, and the above mentioned 2nd unit switch to common timing, a plurality of queuing which stores data which outputs the above mentioned 1st unit switch to the outgoing line corresponding to an output port where the mentioned above separation circuits were connected for every low speed interface, a table which defines a low speed interface which should output multiple address data

when the outgoing line is the outgoing line which connects the mentioned above low speed interface, while defining a plurality of outgoing lines which should output each multiple address data, a multiple address processing means to judge a low speed interface which should output multiple address data by referring to the mentioned above table, and to store multiple address data to queuing corresponding to an applicable low speed interface, from the mentioned above queuing, a selector which controls by identification timing an order which outputs data, and the above mentioned 2nd unit switch, a plurality of queuing which stores data to output for every low speed interface to the outgoing line corresponding to an output port which connected the mentioned above separation circuits, a selector which controls by identification timing a distribution circuit which distributes data inputted from incoming line to queuing corresponding to a low speed interface which should be outputted by the mentioned above identification timing, and an order which outputs data from the mentioned above queuing.

[Claim 12] The data exchange device according to claim 1 characterized by exchanging for a multiple address copy of data corresponding to the mentioned above high speed interface and the above mentioned 2nd unit switch outputs multiple address data corresponding to the mentioned above high speed interface to a plurality of output ports accommodated in the mentioned above high speed interface, the mentioned above data exchange device is provided with a plurality of output ports accommodated in one high speed interface at least, and the above mentioned 1st unit switch.

[Claim 13] The data exchange device according to claim 12 outputting data to each outgoing line in an order which was provided with one queuing which stores data to a plurality of outgoing lines corresponding to a plurality of output ports connected to the mentioned above multiplex circuit, and was stored by the mentioned above queuing, while the mentioned above data exchange device is connected to the latter part of an

output port of further the mentioned above plurality and connecting the mentioned above high speed interface, a multiplex circuit which multiplexes data outputted from a plurality of output ports, and is outputted to the mentioned above high speed interface, and the above mentioned 1st unit switch and the 2nd unit switch.

[Detailed description of the invention]
[0001]
[Industrial application] This invention relates to the data exchange device for which various information on multimedia, including a sound, data, picture, and the like, is exchanged at high speed. In the Asynchronous Transfer Mode (ATM) communication method especially adopted as broadband ISDN, it is related with the cell exchange device for which the cell which is the fixed length packet which blocked these data is exchanged at high speed.
[0002]
[Description of the prior art]
Conventional example 1. When a large scale switch is constituted, a unit switch is made into multistage constitution and the method of aiming at scale extension is known from the former. The case where 3 steps connect with the literature "Examination of ATM exchange system architecture"« (Institute of Electronics, Information and Communication Engineers technical research report SSE89-38-1989. Suzuki, Suzuki, Ito, Sekito), as an example of multistage constitution is published. The composition model of a speech path is shown on drawing 36. The cell which went into the system from the ON circuit is changed to the operation clock of a system from the receive clock on a circuit in a cell synchronization part, and is further outputted according to the cell synchronous timing specified on the speech path in a system. Next, a cell is inputted into a header processing part. Here, if the header check of a cell is performed first and there is no error in a header unit, the outgoing line information

which specifies to which outgoing line of a switch it outputs based on VCI will be added, and it will change into the value which came out of the value of VCI of a header unit further, and was preliminary decided to be circuit correspondence. After performing header conversion, a cell is inputted into an ATM switch part, and switching is performed to the outgoing line specified using the outgoing line information added in the header processing part, and it is outputted. A cell traffic test section measures the through put of a cell, and the like the preceding paragraph of a switch, immediately after, and the like, in order to grasp the state of a speech path or to calculate the traffic for every call. All are required functions although it is not necessarily the physical relationship shown by drawing 36 not necessarily with the way of processing about the arrangement position of each function.

[0003] Next, a header processing part considers the form of the route information given to a switch. Usually, what is necessary is just to give the outgoing line (appearance port) number of each unit switch by the number of stages of a switch in accordance with the course of the route determined as a result of call processing. If the support to a broadcast connection is pondered, expression by the bit map format (Every bit of the outgoing line of a switch correspondence and the value of a bit it is a cell output specification) for which the output to a plurality of outgoing lines can be specified is required. On the other hand, at the time of the usual 1 to 1 connection, how only a broadcast connection uses a bit map format expression can be considered using an outgoing line number. The comparison of the capacity of the route information retrieving table at the time of bit map expression is altogether indicated to be this method to drawing 37. By making bit map format expression only into a multiple address call from a drawing, it turns out that hardware quantity of a table can be made small considerably. A multiple address call changes VCI into a multiple address call identity number once in the header processing part of the switch preceding paragraph, and searches

and bit maps a table from a multiple address call identity number by a switch part. At the time of 1 to 1 connection, an outgoing line number is searched for in the header processing part of the switch preceding paragraph, and it sends to a switch. Next, the VCI update process of a cell is considered. Only after considering a broadcast connection switching (= the duplicate of a cell), renewal of VCI can be performed. However, in order to carry out VCI conversion in the switch latter part, it is necessary to turn with the identification number (a previous multiple address identifier is equivalent to this) for every call which can be replaced with an incoming line number or it to the VCI converter of the switch latter part. Considering using an identifier in the case of the multiple address, at the time of the usual 1 to 1 connection, when searching for the route information of the switch preceding paragraph, the update process of VCI is performed, at the time of a broadcast connection, the method of changing in the header processing part provided in the switch latter part using the multiple address call identity number can lessen the information around which it has and turns, and its table does not increase, either, but it is suitable. The composition of a header processing part based on the above examining result is shown on drawing 38. In the case of a 1 to 1 connection call, after the header processing part arranged at the switch preceding paragraph performs the header check of the inputted cell, searches VCI (new VCI) defined on outgoing line information and the following link from VCI and rewrites VCI, a cell and outgoing line information are sent to a switch part.

[0004] In the case of a broadcast connection call, the header processing part arranged at the switch preceding paragraph searches a multiple address call identity number from VCI, and inputs into a switch with a cell. The cell outputted from the switch is a header processing part arranged at the outputting part of a switch, and search of new VCI is performed and it is written in a header by the multiple address call identity number given previously. Also as shown in drawing 37 as actual composition,

in order that the capacity of each table may exceed 100 Kbytes, under the present circumstances, building in LSI is not a best policy. As access serves as a cell unit, the usual general purpose memory device can be used. Thus, it is appropriate for a header processing part that the table which consists of Boolean part which includes LSI which performs check of a header unit, conversion, and memory control, and a general purpose memory connected to it realizes.

[0005] As mentioned above, while making a unit switch into multistage constitution and constituting a large scale switch, a cell is copied, and it distributes to a plurality of addresses, namely, the multiple address is examined. As shown on drawing 37, simultaneously examination that the quantity of the address bit map table which manages a plurality of the outgoing lines which should be outputted becomes large according to the identification number (VCI value) of the call in incoming line is also carried out. When 3 step connection and the like carry out multi stage connection especially for large scaling, as it is shown on drawing 38, each switch is provided with an address bit map table, and routing to multiple address cells is performed. Thus, although there is a problem used as what has a huge size of an address bit map table, according to the literature, the number of multiple address calls is restricted, the proposal which introduces a multiple address identifier is proposed, and it is shown that address bit map tables are reduced. However, as multiple address cells may arrive from all the incoming line about the 2nd step and the 3rd step, it must have the destination information of the multiple address call of all the incoming line. The multiple address call number gave the number to the multiple address call including all the incoming line, and if the worst, there was a problem of becoming a very large number.

[0006] Conventional example 2. A unit switch is made into 2 stage constitution, and, when a large scale switch is constituted, the method of measuring scale extension is already indicated by the literature «An ATM System and Network Architecture in

Field Trial» (GLOBECOM'93, the session 40, 40.5-1993 year .Wolfgang Fischer, Rolf Stiefel, Tom Worster). The case where the large scale switch of 64x64 is constituted is shown on drawing 39, using the 12 switches of 32x16 . The large scale switch of 64x64 is formed by connecting to 4 set parallel the funnel type structure (A) which constitutes 64x16 by a diagram. A large scale switching network is possible by how to combine everything but a switching element. For example, 3 stage constitution can constitute the switching network of 128x128.

[0007] However, processing the multiple address is not stated in the literature. As it is necessary in the switch after the 2nd step to distribute the cell of all the incoming lines if the same idea as the conventional example 1 is introduced, the problem that the quantity of an address bit map table increases occurs.

[0008] There is an example of JP 4-180433 A of the ATM switch which can accommodate the low speed interface of conventional example 3.

[0009] Drawing 40 is an entire configuration drawing showing a cell exchange device. This cell exchange device 8 exchanges cells among the 32 output ports 7 of 155.52 Mb/s which outputs the 32 input ports 6 and cell of 155.52 Mb/s which a cell inputs. This cell exchange device 8, the cell multiplex circuit 4 which carries out cell multiplex of the input port 6 of 155.52 Mb/s to one incoming line 1 of 622.08 Mb/s circuits, it is 8 circuit preparation about the cell separation circuits 5 which carry out cell separation of ATM switch 3 which accommodates 8 incoming lines 1 and the 8 outgoing lines 2 with a 622.08 Mb/s interface, and the one outgoing line 2 of 622.08 Mb/s in 4 output ports 7 155.52 Mb/s.

[0010] Drawing 41 shows the example of the mentioned above ATM switch 3. In the drawing, 1 is incoming line of n (n>=2) with which cell multiplex of the input port which the cell which consists of a header unit which includes an output port number as destination information, and a data division inputs was carried out. 2 is the outgoing line of m (m>=2) which accommodated the output port where the mentioned above cell should be outputted

according to the address specified in the header unit. 10 is a header processing circuit which detects the output port 7 of an address from the header unit of the cell which was provided corresponding to each of the mentioned above incoming line 1, and was inputted from the incoming line 1. 11 is a buffer memory of p (p>=1) individual which can read the cell which accumulated the mentioned above cell in the specified address and was accumulated regardless of an order in the case of writing by specifying an address. 12 is a storage control circuit which is provided corresponding to each of this buffer memory 11, for example, manages an open address using a FIFO type memory, and gives a read address and a write address to the matched buffer memory 11. 13 is the cell circuit writing which connects the mentioned above header processing circuit 10 to the predetermined buffer memory 11 selectively, and is realized by the space switch. 14 is cell readout circuitry which connects each buffer memory 11 to the predetermined outgoing line 2 selectively, and is realized by the space switch.

[0011] 15 is a buffer control circuit. The buffer control circuit 15 chooses the buffer memory 11 which controls switching of the mentioned above cell circuit writing 13 and in which a cell is accumulated. Switching of the cell readout circuitry 14 is controlled based on the address which managed the address on the buffer memory 11 of the accumulated cell according to the output port of each cell, and has been managed according to the address concerned. And it is outputted to the outgoing line 2 which accommodates the mentioned above output port 7 specified by the header unit in the mentioned above cell in predetermined order.

[0012] The mentioned above buffer control circuit 15 has the following composition. If a cell reaches the incoming line 1, the write buffer selection circuitry 16 will receive the outgoing line number of the cell concerned detected by the header processing circuit 10 provided corresponding to the incoming line 1, and will choose the buffer memory 11 which accumulates the cell. And in

order to connect the buffer memory 11 to the applicable header processing circuit 10, switching of the mentioned above cell circuit writing 13 is controlled. The address exchange circuit 17 divides the cell which arrived with reference to the output port number which this write buffer selection circuitry 16 detected according to the output port of an address, the write address on the buffer memory 11 in which the cell concerned was written is obtained from the storage control circuit 12 corresponding to the buffer memory 11 concerned, and it writes in address queuing which mentions it later. 18 is address queuing, is constituted by the FIFO type memory and provided corresponding to the output port which each of the mentioned above outgoing line 2 accommodates. The write address on the buffer memory 11 by which the cell with which it was matched, and which makes the output port concerned an address for every output port was accumulated in the address queuing 18 is written in the turn which arrived by the mentioned above address exchange circuit 17. The read out buffer selection circuitry 19 determines the cell read from the buffer memory 11 with reference to the address queuing 18, and sends the address read from the address queuing 18 to the storage control circuit 12 matched with the buffer memory 11 applicable as a read address. Switching of the cell readout circuitry 14 is controlled and the mentioned above buffer memory 11 is connected to the applicable outgoing line 2.

[0013] Drawing 42 is an example of an internal circuit of a cell multiplex circuit, and is an example which carries out cell multiplex of the input port 6 of four 155.52 Mb/s to one incoming line 1 of 622.08 Mb/s in drawing 40. Among the drawing, the cell speed adjustment buffer 21 which included 1 FIFO type memory corresponding to the input port 6 is used, and it writes in by 155.52 Mb/s and it is reading by 622.08 Mb/s one by one. Drawing 44 is an example of an internal circuit of cell separation circuits, and is an example which carries out cell separation of the one outgoing line 2 of 622.08 Mb/s in drawing 40 in the output port 7 of four 155.52 Mb/s. Among the drawing, the cell speed

adjustment buffer 23 and the address filter 22 which included 1 FIFO type memory corresponding to the output port 7 are used, and it writes in by 622.08 Mb/s and they are reading by 155.52 Mb/s. As the cell speed adjustment buffers 21, 23 are not what expects the statistic multiplex effect of a cell only for the purpose of speed regulation, the most capacity is enough by a part grade for 2 cells. Next, operation of a cell multiplex circuit is explained. The cell length processed here is fixed length, and it is an inputting at random, before inputting into the input port 6, a cell input phase shall be adjusted, and the cell input from the whole line shall be supplied with the same phase. Drawing 43 is a timing diagram in this example of a circuit, the input port 6 of drawing 42 is set to A, and it sets the incoming line 1 to B, and has shown it by the cell unit, respectively. The case where a significant cell comes to a certain time slot, and an idle cell (empty cell) with no information may come by an ATM communication method. «The cell 1» and the like shows a significant cell in a drawing, and the idle cell (empty cell) is clearly written to be an «idle cell». 1 cell transfer time of 622.08 Mb/s is 1/4 of 155.52 Mb/s. There is capacity which accommodates all the cells inputted from the input port 6 in the incoming line 1. Here, 1 cell time in 155.52 Mb/s was made into the unit, and the method which assigns the input port 6 for 4 cells of 622.08 Mb/s fixed in the time position is taken. For example, it is made to output the cell inputted from the input port 6 of #1 as 622.08 Mb/s in the position of #1 in a drawing.

[0014] Next, operation of an ATM switch is explained about drawing 41. Here, the input phase of the cell in each incoming line 1 inputted into a switch is adjusted, and is taken as the same. If a cell inputs into the incoming line 1, the header processing circuit 10 provided corresponding to each incoming line 1 will detect the outgoing line number which accommodates an output port and it from the header unit of the inputted cell. The write buffer selection circuitry 16 in the buffer control circuit 15 directs to connect separately the buffer memory 11 chosen in order to

store the header processing circuit 10 and cell to which the cell arrived at the cell circuit writing 13 with reference to this header processing circuit 10. The write address used at this time is obtained by referring to the storage control circuit 12. This write address is sent to the address exchange circuit 17, and is divided according to the address output port 7 of the cell which reached each incoming line 1.

[0015] The address queuing 18 is established according to an output port, and the write address and buffer memory number of the mentioned above cell are written in the tail end. While sending the read out buffer selection circuitry 19 to the storage control circuit 12 corresponding to the buffer memory 11 which takes out the address stored there from these address queuing 18, and corresponds, it directs to connect the buffer memory 11 and the outgoing line 2 separately to the cell readout circuitry 14. As read out of the address queuing 18 is performed per output port, it is made not to exceed the capacity of the output port 7 by reading according to the speed of an output port, although the capacity of the outgoing line 2 generally differs from the capacity of the output port 7. The cell readout circuitry 14 connects the outgoing line 2 with the buffer memory 11 in this time slot. Each storage control circuit 12 is sent to the buffer memory 11 which had the received address matched as a read address, and manages the address as an open address next. The cell read from each buffer memory 11 is outputted to the outgoing line 2 that accommodates the address output port 7 specified by each header unit.

[0016] Here, drawing 46 and drawing 47 are the examples which showed read out of the address queuing 18 about outgoing line #1 in detail. As outgoing line #1 has accommodated output port #1 - #4 of 155.52 Mb/s, It includes the speed of 622.08 Mb/s. Drawing 46 is an example of the address queuing 18 corresponding to output port #1 - #4 in a certain time slot. The buffer memory number and address which store the cell are written in the place indicated to be «the cell 11» and the like. Drawing 47 shows the read out rule of the address queuing 18. The drawing shows the

timing in the outgoing line 2. It differs from the former in that the cell addressed to output port #1 - #4 is assigned to 4 cell units fixed, respectively. For example, the time slots 1-4 are assigned among a drawing to output port #1 - #4, respectively, and it is repeated. Thus, in the cell separation circuits 5, what is necessary is to perform only speed regulation regularly, and the cell abolition by the buffer overflow in the cell separation circuits 5 does not arise. For example, in drawing 46, the cell 41 is waiting for the output to present output port #1 at the cell 21 and addressing to #4 at the cell 11 and addressing to #2. Thus, they are regularly read by the time slots 1, 2, and 4. In the time slot 3, as the cell addressed to output port #3 has not arrived, the idle cell («empty cell» in drawing and specification) has been sent out.
[0017] Although the address queuing 18 is established corresponding to the output port 7, it is thought that there is one big queuing to the outgoing line 2 in the conventional example, as other significant cells will be outputted by the time slot 3 if this example is applied, an empty cell will not be outputted, output port #1, #2 or #4 will overlap, and it is necessary to buffer in the cell separation circuits 5. That is, in the conventional example, to the one output port 7, statistical fluctuation will occur in arrival of a cell, it takes a lot of buffers in the cell separation circuits 5.
[0018] Next, operation of cell separation circuits is explained. Drawing 45 is a timing diagram in this example of a circuit. The outgoing line 2 of drawing 44 is set to C, the output port 7 is set to D, and the cell unit has shown, respectively. Like drawing 43 in a drawing, «the cell 1» and the like shows a significant cell and the idle cell (empty cell) is clearly written to be an «idle cell». The transfer time of 622.08 Mb/s is 1/4 in 155.52 Mb/s. Although the outgoing line 2 transmitted from ATM switch 3 is 622.08 Mb/s, as 1 cell time in 155.52 Mb/s is made into a unit and the output port 7 is assigned for four cells of 622.08 Mb/s fixed in the time position, the output port 7 and time slot which certainly output the cell inputted into the cell separation circuits 5 are guaranteed, and buffer overflow is produced. The multiple

address of the cell inputted into the cell separation circuits 5 is carried out to the address filter 22 first provided corresponding to the output port 7, and only the address filter 22 corresponding to the corresponding output port 7 passes the mentioned above cell, and writes it in the speed regulation buffer 23. The mentioned above cell is discarded in other address filters 22. Speed regulation is performed by writing performing the cell speed adjustment buffer 23 by 622.08 Mb/s, and performing read out by 155.52 Mb/s. as the cell speed adjustment buffer 23 is not what expects the statistic multiplex effect of a cell only for the purpose of speed regulation, most capacity is enough by a part grade for 2 cells.

[0019] However, as only the case where a switch was one step was considered in the mentioned above case, there was a problem that a large scale switch could not be constituted. Realization of the multiple address function was not described, either.

[0020] Conventional example 4. Compared with incoming line and the outgoing line of a ATM switch, «Development of common buffer type ATM switch LSI with a multiple address function» (Institute of Electronics, Information and Communication Engineers, Shingaku Giho SSE92-169-1993) is indicated about the system which accommodates a high speed interface.

[0021] As shown on drawing 48, a 2.4 Gb/s circuit is accommodated by connecting MUX to incoming line #0 - 3 of a unit switch DMUX and outgoing line #0 - 3. At this time, within a unit switch, queuing of the cell to outgoing line #0 - 3 is carried out to one address queue, and order management of a cell is performed. Also by DMUX, an order of a cell can be maintained by outputting to incoming line #0 - 3 sequentially from the cell received previously, and sending out a cell to a circuit in order of outgoing line #0 - 3 in MUX. In addition, it is possible to connect ON / outgoing line #4 - 7, and to choose and accommodate either 600 Mb/s 4 circuit or 150 Mb/s 16 circuit in this.

[0022] However, as only the case where a switch was one step was considered, there was a problem that a large scale switch could not be constituted.
[0023]
[Problems to be solved by the invention] This invention was made in order to solve above problem, it makes a unit switch multistage constitution, and measures a scale expansion, and an object of an invention is to obtain the data exchange device which can process multiple address data efficiently simultaneously.
[0024] This invention carries out multistage constitution of the unit switch, and an object of an invention is to obtain the data exchange device which can measure a scale expansion and can accommodate a plurality of low speed interfaces.
[0025] An object of this invention is to obtain the data exchange device which can make a unit switch multistage constitution, and can measure a scale expansion, and can accommodate a high speed interface.
[0026]
[Means for solving the problem] A data exchange device according to the 1st invention is provided with a plurality of input ports and a plurality of output ports, and between a plurality of input ports and a plurality of output ports, in a data exchange device which arranges a plurality of unit switches which exchange data between a plurality of incoming lines and a plurality of outgoing lines to at least 2 steps and for which data is exchanged between a plurality of input ports and a plurality of output ports, making a unit switch of the 1st step into the 1st unit switch, and a unit switch after the 2nd step is made into the 2nd unit switch, if a plurality of 1st unit switches have necessity from a certain input port to inputted multiple address data, while exchanging for a multiple address copy of data and outputting a plurality of copied multiple address data to the outgoing line corresponding to an output port of the multiple address point, respectively, the 2nd unit switch inputs copied multiple address data which has a plurality of unit switches in the preceding

paragraph, and is outputted to it from the outgoing line of a plurality of unit switches of the mentioned above preceding paragraph, a multistage connection part exchanging inputted copied multiple address data based on a predetermined rule defined preliminary, and outputting to an output port of the multiple address point eventually.

[0027] A data exchange device according to the 2nd invention branches and inputs into a plurality of the mentioned above multistage connection parts data into which the mentioned above multistage connection part was inputted in a plurality of preparations and an input port, and an output port which is different in the mentioned above multistage connection part, respectively is assigned.

[0028] In a data exchange device according to the 3rd invention, the above mentioned 1st unit switch, a multiple address processing means which judges the outgoing line which should output multiple address data, and is exchanged for a multiple address copy of data by referring to a table which defined a plurality of outgoing lines which should output each multiple address data, and the mentioned above table.

[0029] In a data exchange device according to the 4th invention, the above mentioned 2nd unit switch determines the outgoing line which outputs copied multiple address data based on an incoming line number of incoming line which inputs copied multiple address data.

[0030] A data exchange device according to the 5th invention is a cell exchange device for which a cell with a virtual path identifier and a virtual channel identifier is exchanged, defining the mentioned above table and a plurality of outgoing lines which should output multiple address cells to a virtual path identifier and a virtual channel identifier the above mentioned 1st unit switch, the outgoing line which should be carried out the multiple address from the mentioned above table based on a virtual path identifier and a virtual channel identifier of multiple address cells is determined.

[0031] In a data exchange device according to the 6th invention, the mentioned above table is independently provided to each 1st unit switch, respectively.
[0032] In a data exchange device according to the 7th invention, the mentioned above table is provided in common to a plurality of 1st unit switches.
[0033] A data exchange device according to the 8th invention is a cell exchange device for which a cell is exchanged, a cell exchange device is provided with a multiple address identifier allocation means which assigns a multiple address identifier which identifies multiple address cells in the preceding paragraph of an input port to each multiple address cells, the mentioned above table defines the outgoing line which should output multiple address cells to a multiple address identifier, and the above mentioned 1st unit switch determines the outgoing line which should be carried out the multiple address from the mentioned above table based on a multiple address identifier.
[0034] In a data exchange device according to the 9th invention, the mentioned above multiple address identifier allocation means is established to an incoming line group which includes a plurality of the mentioned above input ports, respectively.
[0035] A data exchange device according to the 10th invention is provided with an output port in which a plurality of low speed interfaces are accommodated, and the above mentioned 1st unit switch, exchanging for a multiple address copy of data corresponding to a plurality of the mentioned above low speed interfaces, the above mentioned 2nd unit switch outputs multiple address data corresponding to a plurality of the mentioned above low speed interfaces to an output port in which a plurality of the mentioned above low speed interfaces are accommodated.
[0036] A data exchange device according to the 11th invention is connected to the latter part of one of the mentioned above output ports further at least and connecting a plurality of low speed interfaces, separation circuits which separate data outputted from the output port, and are outputted to the mentioned above low

speed interface, a timing generating means which generates identification timing for operating the mentioned above separation circuits, the above mentioned 1st unit switch, and the above mentioned 2nd unit switch to common timing, while the above mentioned 1st unit switch defines a plurality of queuing which stores data to output for every low speed interface, and a plurality of outgoing lines which should output each multiple address data to the outgoing line corresponding to an output port where the mentioned above separation circuits were connected, by referring to a table which defines a low speed interface which should output multiple address data, and the mentioned above table, when the outgoing line is the outgoing line which connects the mentioned above low speed interface, judging a low speed interface which should output multiple address data, a multiple address processing means to store multiple address data to queuing corresponding to an applicable low speed interface, and a selector which controls by identification timing an order which outputs data from the mentioned above queuing, and the above mentioned 2nd unit switch, a plurality of queuing which stores data to output for every low speed interface to the outgoing line corresponding to an output port which connected the mentioned above separation circuits, a selector which controls by identification timing a distribution circuit which distributes data inputted from incoming line to queuing corresponding to a low speed interface which should be outputted by the mentioned above identification timing, and an order which outputs data from the mentioned above queuing.

[0037] A data exchange device according to the 12th invention is provided with a plurality of output ports accommodated in one high speed interface at least, and the above mentioned 1st unit switch, exchanging for a multiple address copy of data corresponding to the mentioned above high speed interface, the above mentioned 2nd unit switch outputs multiple address data corresponding to the mentioned above high speed interface to a

plurality of output ports accommodated in the mentioned above high speed interface.
[0038] According to the 13th invention a data exchange device is connected to the latter part of an output port of the mentioned above plurality and connecting the mentioned above high speed interface, a multiplex circuit which multiplexes data outputted from a plurality of output ports, and is outputted to the mentioned above high speed interface, and the above mentioned 1st unit switch and the 2nd unit switch, 1 queuing which stores data to a plurality of outgoing lines corresponding to a plurality of output ports connected to the mentioned above multiplex circuit, and data is outputted to each outgoing line in an order stored by the mentioned above queuing.
[0039]
[Function] The data exchange device in the 1st invention is provided with a plurality of 1st unit switches and a plurality of 2nd unit switches. A data exchange device will be the 1st step from a plurality of 1st unit switches and the multistage connection part which has arranged a plurality of 2nd unit switch after the 2nd step. It is connected to an input port, and if incoming line of the 1st unit switch has necessity, it will perform a multiple address copy of data. And a plurality of copied multiple address data is outputted to the outgoing line corresponding to the output port of the multiple address point, respectively. The 2nd unit switch is arranged after the 2nd step. The 2nd unit switch arranged in the 2nd step inputs copied multiple address data from a plurality of 1st unit switches of the preceding paragraph. And the outgoing line is determined based on the predetermined rule defined preliminary. If there is the 4th step..., from the 2nd unit switch of the preceding paragraph, the 2nd unit switch will input copied multiple address data, and will determine the 3rd step of outgoing line based on the predetermined rule defined preliminary. And it is connected to the output port and the outgoing line of the 2nd unit switch of a final stage outputs copied multiple address data to the output port of the multiple

address point. By using a plurality of 1st unit switch, the number of input ports which can connect with a data exchange device can be increased.

[0040] The data exchange device in the 2nd invention is provided with a plurality of multistage connection parts which carried out multi stage connection of a plurality of the 1st unit switch and 2nd unit switch. The data inputted into the input port is branched and inputted into a plurality of the mentioned above multistage connection parts. And an output port different, respectively is assigned to a multistage connection part. Thus, the number of output ports which can connect with a data exchange device can be increased.

[0041] The data exchange device in the 3rd invention equips the 1st unit switch with the table which defined a plurality of outgoing lines which should output each multiple address data. By referring to the mentioned above table, the multiple address processing means of the 1st unit switch judges the outgoing line which should output multiple address data, and exchanges it for a multiple address copy of data.

[0042] The data exchange device in the 4th invention has the 2nd unit switch that determines the outgoing line which outputs the inputted copied multiple address data based on an incoming line number. Thus, it is not necessary to have a table for determining the outgoing line of the inputted data in the 2nd unit switch.

[0043] The data exchange device in the 5th invention is a cell exchange device for which a cell with a virtual path identifier and a virtual channel identifier is exchanged. The table with which the 1st unit switch is equipped defines a plurality of outgoing lines which should output multiple address cells to a virtual path identifier and a virtual channel identifier. Thus, the 1st unit switch can determine the outgoing line which should be carried out the multiple address from the mentioned above table based on the virtual path identifier and virtual channel identifier of multiple address cells.

[0044] The data exchange device in the 6th invention is independently provided with the table which determines destination outgoing lines for every unit switch. Thus, as a table should just be aimed only at the multiple address data inputted from the input port connected to each 1st unit switch, it can make the size of a table small.
[0045] 1 table can be shared and used for the data exchange device in the 7th invention by a plurality of 1st unit switches. Or all the 1st unit switch can use 1 table too.
[0046] The data exchange device in the 8th invention is a cell exchange device for which a cell is exchanged. A cell exchange device has a multiple address identifier allocation means. It is connected to the preceding paragraph of an input port, and a multiple address identifier allocation means assigns the multiple address identifier which identifies multiple address cells to each multiple address cells. The mentioned above table defines the outgoing line which should output multiple address cells to a multiple address identifier. The 1st unit switch determines the outgoing line which should be carried out the multiple address from the mentioned above table based on a multiple address identifier.
[0047] The data exchange device in the 9th invention divides the input port into the incoming several and every line group. A multiple address identifier allocation means is established to each incoming line group. Thus, the number of the multiple address identifiers which need to be registered into a table is easy to come out about the multiple address data inputted from the input port belonging to a corresponding incoming line group. Thus, the size of a table can be made small.
[0048] The data exchange device in the 10th invention can accommodate a plurality of low speed interfaces in an output port. The 1st unit switch exchanges for the multiple address copy of data corresponding to the case where an output port is equipped with a plurality of low speed interfaces. The 2nd unit

switch outputs the multiple address data corresponding to a plurality of the mentioned above low speed interfaces.
[0049] The data exchange device in the 11th invention can accommodate a low speed interface in the latter part of an output port. A low speed interface is connected to the output port of a data exchange device by separation circuits. A data exchange device is provided with a timing generating means. A timing generating means generates the identification timing for operating the mentioned above separation circuits, the 1st unit switch, and the 2nd unit switch to common timing. The 1st unit switch has a plurality of queuing which stores the data outputted to the outgoing line corresponding to the output port connected to the mentioned above separation circuits for every low speed interface. The table with which the 1st unit switch is equipped defines a plurality of outgoing lines which should output multiple address data. When the outgoing line is the outgoing line which connects the mentioned above low speed interface, the low speed interface which outputs multiple address data is defined. The multiple address processing means of the 1st unit switch judges the low speed interface which should output multiple address data with reference to the mentioned above table, and stores multiple address data to queuing corresponding to the low speed interface. When outputting data from a plurality of queuing corresponding to a low speed interface, a selector outputs data from which queuing or controls it by identification timing. The 2nd unit switch has a plurality of queuing which stores the data outputted the whole low speed interface, when it is the outgoing line corresponding to the output port which connected the mentioned above separation circuits. It has a distribution circuit which distributes the data inputted from incoming line to queuing corresponding to a low speed interface by the mentioned above identification timing. The selector of the 1st unit switch and the distribution circuit of the 2nd unit switch are controlled by the same identification timing. The data stored by this by queuing corresponding to one low speed interface with the 1st unit switch

will be stored by queuing corresponding to the same low speed interface of the 2nd unit switch. That is, a synchronization can be taken between the 1st unit switch and the 2nd unit switch by giving the same identification timing. It includes the selector which controls by the mentioned above identification timing an order which outputs data from queuing corresponding to a low speed interface. As the 2nd selector and separation circuits of a unit switch are controlled by the same identification timing, when data is separated for every low speed interface in separation circuits, data is correctly outputted to the low speed interface of an address. Compared with the output from queuing corresponding to the usual outgoing line, the number of times of the data outputted from a plurality of queuing stored for every low speed interface has decreased by equipping the 1st, 2nd unit switch with a selector. Thus, the cell abolition by buffer overflow in separation circuits can be lost.

[0050] The data exchange device in the 12th invention accommodates at least 1 high speed interface in an output port. It is connected to 1 high speed interface in a plurality of output ports. The 1st unit switch exchanges for the multiple address copy of data corresponding to a high speed interface. The 2nd unit switch can output the multiple address data corresponding to a high speed interface to a plurality of output ports accommodated in the mentioned above high speed interface.

[0051] The data exchange device in the 13th invention connects a multiplex circuit to the latter part of a plurality of output ports, and connects a high speed interface to the latter part of this multiplex circuit. A multiplex circuit multiplexes the data outputted from a plurality of output ports. The 1st unit switch and 2nd unit switch are provided with 1 queuing which stores data to a plurality of outgoing lines corresponding to a plurality of output ports connected to the mentioned above multiplex circuit. In the order stored by the mentioned above queuing, data is outputted to each outgoing line.

[0052]

[Example]
Example 1. In this example, a large scale ATM switch is constituted, an example of a method which makes a unit switch multistage constitution and aims at scale extension is explained. Although the topology explained in this example is based on the connection method indicated to the conventional example 2, it is the concentrated type conjunctive of lines from which the function of the 1st step and the switch after it differed. For example, when 2 steps connect, the copy and exchange of a cell are performed by the first step of unit switch, and the second step of unit switch judges an address from the incoming line number information which the cell inputted.
[0053] The number of incoming line connects 8, the number of the outgoing lines connects 2 steps of unit switches of 2 (it is next described as 8x2) on drawing 1, and the example from which the number of input ports constitutes 32 and the number of output ports constitutes the large scale switch of 32 (it is next described as 32x32) is shown on it. In drawing 1, S1-1 - S1-4 is the 8x2 1st unit switch. T-1 to T-4 is the address bit map table which defined a plurality of outgoing lines which output multiple address cells. S2-1 is the 8x2 2nd unit switch. In the following examples, about incoming line of the 1st unit switch S1 and the 2nd unit switch S2, incoming line of the incoming line number i (i= 0, 1, 2, ...) is called the incoming line i, and the outgoing line of the outgoing line number outgoing line i is called the outgoing line i (i= 0, 1, 2, ...). The 1st incoming line of unit switch S1-1 is connected to input port #0 - #7, respectively. The 1st unit switch S1-2, S1-3, S1-4 are similarly connected to #8-#15, #16-#23, #24 - #31, respectively. The 1st outgoing line 0 and 1 of unit switch S1-1 is connected to the incoming line 0 and 1 of 2nd unit switch S2-1 from a top, respectively. The outgoing lines 0 and 1 of other 1st unit switch S1-2, S1-3, S1-4 are similarly connected to the incoming line 2 and 3 of 2nd unit switch S2-1, 4, 5, 6 7, respectively. The two outgoing lines 0 and 1 of 2nd unit switch S2-1 are connected to output port #0 and #1. The 1st unit switch

S1-1 - S1-4 is provided with the address bit map table T-1 to T-4, respectively. The 1st unit switch S1-1 judges a plurality of addresses with reference to the address bit map table T-1 from the header information of the multiple address cells inputted into input port #0 - #7. If there is a plurality of addresses, multiple address cells will be copied, and a cell is outputted to the outgoing line shown on the address bit map table T-1. The 2nd unit switch S2-1 judges an address using an incoming line number. Thus, the address bit map table is unnecessary.

[0054] P-1 to P-16 is a multistage connection part. The multistage connection part P-1 to P-16 includes a unit switch group which carried out multi stage connection of four pieces and the 2nd unit switch S2 to one piece and the concentrated type of lines in the 1st unit switch S1. The signal from input port #0-#31 is branched and inputted into the multistage connection part P-1 to P-16. That is, a cell with the multistage connection part P-1 and the multistage connection part P-2... P-16 same from input port #0-#31 is inputted. Output port #0 and #1 are assigned to the multistage connection part P-1, and output port #2 and #3 are assigned to the multistage connection part P-2. Thus, the multistage connection part P assigns 32 input ports and 2 output ports (32x2). And it can have a total of 32 output ports by assigning every 2 different output ports to the multistage connection part P of 16, respectively. It is possible to constitute the large scale switch of 32x32 by the above composition, using a plurality of the unit switch of 8x2.

[0055] Drawing 2 is a block diagram of the 1st unit switch S1. As the component of the same number as the conventional example 3 has the same work in a drawing, explanation is omitted. 131 is a header processing circuit. The header processing circuit 131 holds the cell which reached incoming line, and reads the header information of a cell. The write buffer selection circuitry 111 receives the header information of the cell read by the header processing circuit 131, and judges an address, namely, an outgoing line number, with reference to the address bit map table

T. Without an address, a cell is discarded and future processings are not performed. When there are one or more addresses, the write buffer selection circuitry 111 chooses the buffer memory 11 which stores a cell, and connects the header processing circuit 131 and the buffer memory 11 by the switching control of the cell circuit writing 13.

[0056] A1-0, A1-1 are address queuing. The address queuing A1 is established corresponding to the outgoing line, and is constituted by the FIFO type memory. Address queuing A1-0, A1-1 correspond to the outgoing lines 0 and 1, respectively. The write address (address) of the buffer memory 11 where the cell outputted to the outgoing line 0 was stored is written in by the address exchange circuit 120 below mentioned to arrival order. Here, when there is a plurality of outgoing lines of the multiple address point, the address of an applicable cell is written in multi address queuing corresponding to the outgoing line.

[0057] The address exchange circuit 120 writes the address of the buffer memory 11 which stored the cell outputted to the applicable outgoing line in the address queuing A1 corresponding to an outgoing line number. The address of the buffer memory 11 is obtained by the storage control circuit 12 corresponding to the buffer memory 11. An outgoing line number is acquired from the write buffer selection circuitry 111. The multiple address processing means 105 consists of the write buffer selection circuitry 111, the address exchange circuit 120, the address queuing A1, the read out buffer selection circuitry 19, and the address bit map table T.

[0058] Next, operation of the 1st unit switch S1 is explained using drawing 3 - drawing 5. Drawing 3 is a drawing showing the example of operation in the 1st unit switch S1-1. The 1st incoming line 0-7 of unit switch S1-1 assigns input port #0 - #7, respectively. The outgoing lines 0 and 1 are eventually outputted to output port #0 and #1 by the 2nd unit switch S2-1, respectively. The write buffer selection circuitry 111 determines the address which should be outputted with the address bit map table T-1

from the header information of multiple address cells. The address bit map table T-1 to T-4 receives the value of the header information of multiple address cells, expression by the bit map format (each bit corresponding to the outgoing line of a switch, if the value of a bit is «0», there is no cell output, if the value of a bit is «1», it will carry out a cell output) which directs a plurality of destination outgoing lines is taken.

[0059] The multistage connection part P-0 to which the 1st unit switch S1-1 belongs, as #0 and #1 are assigned as a final output port, the address bit map table T-1 should have only the information about whether it outputs to output port #0 and #1 eventually about the multiple address point of multiple address cells. Thus, the size of the address bit map table T-1 of output port #0-#31 as it is not necessary to have all data, it is possible to make small the storage capacity for the address bit map table T-1. As the header information which is an object of the address bit map table T-1 requires only the header information of the multiple address cells inputted into input port #0 - #7, it does not need to have the header information which may be inputted into input port #0 - #31. Thus, the size of an address bit map table may be small compared with the case where all the input ports are taken into consideration. As the size of the address bit map table T-1 is small, there is an advantage that search time is short. As the size of the address bit map table T can be made small, it becomes possible to make RAM store and to build in the 1st unit switch.

[0060] The operation in the 1st unit switch S1-1 when multiple address cells with the header information a and b are inputted from input port #0 and #5 is described. The header processing circuit 131 connected with input port #0, namely, incoming line 0, investigates the header information of the inputted multiple address cells, obtains header information a, and notifies it to the write buffer selection circuitry 111. The write buffer selection circuitry 111 judges the outgoing line 1 from the bit of the outgoing line 1 being «1» with reference to the address bit map

table T-1 to be an address. The address exchange circuit 120 obtains the address of the buffer memory 11 which acquired the outgoing line number and with which the applicable cell was written in from the write buffer selection circuitry 111 from the storage control circuit 12. The address exchange circuit 120 writes a corresponding address in address queuing A1-1 corresponding to the outgoing line 1.

[0061] Next the header processing circuit 131 investigates the header information of the multiple address cells inputted from input port #5, and b is obtained. The write buffer selection circuitry 111 judges with addresses being the outgoing lines 0 and 1 with reference to the address bit map table T-1 from header information b. The address exchange circuit 120 writes an address in address queuing A1-0, A1-1 corresponding to the outgoing lines 0 and 1. One cell of applicable cells is stored to the buffer memory 11, and write the address in 2 address queuing corresponding to the outgoing line. The amount of the buffer memory 11 used to be used can be reduced by this, and management of destination outgoing lines can also be performed. The read out buffer selection circuitry 19 reads an address from address queuing A1-0, A1-1 by FIFO one by one. In the case of drawing 3, header information reads the address of the cell (it is next called the cell b) of b from address queuing A1-0, and it sends to the storage control circuit 12 matched with the applicable buffer memory 11. And switching of the cell readout circuitry 14 is controlled and the cell b is read from the applicable buffer memory 11 to the outgoing line 0. Next, processing with the same the mentioned above of the cell a of address queuing A1-1 is performed, and it outputs to the outgoing line 1. As the read out buffer selection circuitry 19 does not have again a cell which reads address queuing A1-0 although it goes to reading, it outputs an idle cell to the outgoing line 0. Next, the read out buffer selection circuitry 19 goes address queuing A1-1 to reading again, and outputs the cell b to the outgoing line 1. At this time, the address of the buffer memory 11 which stored the cell b is

released. About the release timing of the used address, it has realized by the technique of using a multiple address cell counter (reference: JP 04-175034 A public relations).

[0062] Drawing 4 is a drawing showing the example of operation in the 1st unit switch S1-3. Input port #16 - #23 are connected to incoming line 8, the 1st unit switch S1-3, respectively. The outgoing line passes 0, 1 passes the 2nd unit switch S2-1, and it corresponds to output port #0 and #1. As the address bit map table T-3 corresponds to the same output port #0 and #1 as the address bit map table T-1, it may be a table of the same value. But, as a corresponding input port is different, the address bit map table T-1, T-3 are good also as a table to different header information. As shown, for example in drawing 3 and drawing 4, the value of the outgoing line to the same header information d may be changed. As the address bit map table T is divided and it had it every unit switch S1, it not only can make small the size of the address bit map table T, but it can give a different value. As a partial change of the address bit map table T also divides and has a table, it can carry out easily.

[0063] Supposing that multiple address cells were inputted into the 1st unit switch S1-3 from input port #17, #20, #22 in drawing 4. The 1st unit switch S1-3 investigates the header information of the inputted multiple address cells, when header information is c, gets to know that there are no destination outgoing lines from the address bit map table T-3, and cancels the inputted cell. As the addresses about header information c are 0 and 0 in the address bit map table T-3, the data about header information c may be excluded. In that case, it is good though the cell inputted noting that the information about header information c did not exist in the address bit map table T-3 is canceled. However, in this example, the information about header information c is registered in consideration of a next change. The outgoing lines with which header information should output the multiple address cells of b from the address bit map table T-3 are 0 and 1 and the judging is carried out. And the cell b is stored to the buffer memory 11, and

the address is written in address queuing A1-0 corresponding to the outgoing lines 0 and 1, and A1-1. Header information processes similarly the cell which is d.
[0064] Drawing 5 is a drawing showing the example of the operation in the 1st unit switch S1-63. The cell of the same input port #16 - #23 as the mentioned above S1-3 is inputted into the 1st unit switch S1-63. The 1st unit switch S1-63 is a switch belonging to the multistage connection part P-16. Thus, the outgoing lines 0 and 1 of 1st unit switch S1-63 correspond to output port #30 and #31 by the 2nd unit switch S2-1. It is specified by bit map format whether multiple address cells output eventually the address bit map table T-63 to output port #30 and #31. The 1st unit switch judges the address of multiple address cells b, c, d inputted with reference to the address bit map table T-63. Multiple address cells c and d are outputted to the outgoing line 0. Multiple address cells b is outputted to the outgoing line 1.
[0065] Drawing 6 is a block diagram of the 2nd unit switch S2. Only a different component from drawing 2 is described. The header processing circuit 132 holds the cell which arrived from the unit switch of the preceding paragraph, investigates header information, and judges whether it is an idle cell. In the case of an idle cell, processing does not continue. If it is not an idle cell, an incoming line number will be notified to the write buffer selection circuitry 112. The write buffer selection circuitry 112 determines an outgoing line number from the notified incoming line number. The address queuing A2 is the same as the address queuing A1.
[0066] Drawing 7 is a drawing for explaining operation of the 2nd unit switch S2. The 2nd unit switch judges an address using an incoming line number. Thus, the address bit map table T is unnecessary. In the example shown on drawing 7, the address of the cell which reached the 2nd unit switch S2-1 is taken as just because it divided the incoming line number by the number of the outgoing lines of the 2nd unit switch. In this case, let incoming line 8 of 2nd unit switch S2-1, and the incoming line numbers 0-7. The incoming line 0 and 1 is connected to the 1st unit switch

S1-1. Connect the incoming line 2 and 3 to the 1st unit switch S1-2, the incoming line 4 and 5 is connected to the 1st unit switch S1-3, and the incoming line 6 and 7 is connected to the 1st unit switch S1-4. But, if the connection method of the outgoing line of the 1st unit switch and incoming line of the 2nd unit switch is changed, the outgoing line of the 2nd unit switch can be determined by other methods. For example, the outgoing line 0 of 1st unit switch S1-1 - S1-4 is connected to the incoming line 0-3 of the 2nd unit switch. The outgoing line 1 of 1st unit switch S1-1 - S1-4 is connected to the incoming line 4-7 of the 2nd unit switch. In this case, the cell which outputs the cell to which how to decide the outgoing line by the number of incoming line reaches the incoming line 0-3 of the 2nd unit switch to the outgoing line 0, and reaches the incoming line 4-7 is good also as what is outputted to the outgoing line 1. The outgoing lines 0 and 1 of 2nd unit switch S2-1 are connected to output port #0 and #1. Address queuing A2-0 stores the outgoing line 0, namely, the address of the cell of the waiting for the output of output port #0. Address queuing A2-1 stores the address of the cell of the waiting for the output to the outgoing line 1.

[0067] For example, the cell which reached the incoming line 2 has it judged in the header processing circuit 132 whether it is an idle cell. If it is not an idle cell, the incoming line number 2 will be notified to the write buffer selection circuitry 112. The write buffer selection circuitry 112 calculates 0 just because it broke the incoming line number 2 of the cell by the two outgoing lines, and it determines that destination outgoing lines are 0. The write buffer selection circuitry 112 connects the header processing circuit 132 and the buffer memory 11 by switching of the cell circuit writing 13, and makes the buffer memory 11 store an applicable cell. The address of the buffer memory 11 with which the number of destination outgoing lines was notified from the write buffer selection circuitry 112, and the cell was stored from the storage control circuit 12 is notified to the address exchange circuit 120. The address exchange circuit 120 writes an address in

address queuing A2-0 corresponding to the outgoing line 0. On the other hand, the read out buffer selection circuitry 19 is read from the address of the head of address queuing A2-0, and the storage control circuit 12 is informed about it. And switching of the cell readout circuitry 14 is controlled, the buffer memory 11 and the outgoing line 0 are connected, and the cell of a corresponding address is outputted to outgoing line 0, namely, output port #, 0. It is outputted to the outgoing line 0 through the same processing also about the cell which reached the incoming line 0, 4, 6. The cell that reached the incoming line 1, 3, 5, 7 is outputted to the outgoing line 1.

[0068] By the 2nd unit switch S2, the incoming line number is performing fixed routing processing as mentioned above, and the address bit map table T is the feature of an unnecessary point. For this reason, the total amount of the address bit map table T can be decreased with the whole switch which carried out multistage constitution of the unit switch. The point of having lost cell abolition is the feature by assigning the address of the cell which should output plurality to the address queuing A2 corresponding to the same output port. Although the address of the cell which arrived is carried out to just because it divided that incoming line number by the number of the outgoing lines in this example, it may be determined by other methods that the address stated previously. The above carries out the work also with the 2nd same unit switch in other stage terminal areas, although the 2nd unit switch S2-1 in the multistage connection part P-1 was described as an example. In the case of other multistage connection parts, it differs in that the output port assigned is different, respectively.

[0069] In 3 step connection of the conventional example 1, the address bit map table is arranged to each unit switch of each stage. However, in this example, an address bit map table is put only on the first step of 1st unit switch. In the 2nd unit switch, the point that the incoming line number is performing fixed routing processing for the address of the cell which arrived is the feature.

For this reason, an address bit map table becomes unnecessary at the 2nd unit switch. Thus, the total amount of an address bit map table is reducible with the whole switch which carried out multistage constitution. And as it has an address bit map table for every unit switch, an address which is different to the same header information on each table can also be specified. As an address bit map table can be exchanged for every unit switch, destination management of multiple address cells can be performed more flexibly. Thus, it can tie to a large number of input ports by combining many 1st unit switch with small incoming line and number of the outgoing lines. A large number of output ports can be broken by breaking a plurality of usage and an output port which is alike, respectively and is different, and applying the multistage connection part constituted by a plurality of unit switches.

[0070] Preferential control can be used like the independent case where it is not considered as multistage constitution, in each unit switch.

[0071] Example 2. In this example, 2 steps of unit switches of mxn are connected, and the example which constitutes the large scale switch of MxN is shown.

[0072] Drawing 8 is a line block diagram of the MxN switch according to 2 step connection using the unit switch of mxn. In a drawing, the number of input ports is M. Incoming line of the 1st unit switch S1 is m, and the outgoing line is n. Thus, it connects mM of an input port at a time to 1st unit switch S1-1 - S1-M/m, respectively. Incoming line of the 2nd unit switch S2 is m, and the outgoing line is n. The multistage connection part P has an input port of M, and an output port of n. The number of output ports is N. The multistage connection part P-1 - P-N/n share n output port N books at a time and connect. The address bit map table T is prepared for the 1st unit switch S1, respectively. The address bit map table T of the 2nd unit switch S2 is unnecessary in order to ask for the address of a cell which arrived from the incoming line number. Work of the 1st unit switch S1 and the 2nd

unit switch S2 only differs in the number of incoming line and the outgoing lines, and is the same as that of the mentioned above example. It is the same as that of the mentioned above example also about an address bit map table.

[0073] Here, although the number of the 1st unit switches S1 serves as a M/m individual, when M cannot divide among m, it is considered as below a small number of point up valuation. As the n outgoing lines of the 1st unit switch S1 of a M/m individual are connected at a time to the incoming line m of the 2nd unit switch S2, the relation of m2=nM is realized between M, m, n. The number of the multistage connection parts P is N/n. Here, when N cannot divide among n, below a small number of point shall revalue.

[0074] Drawing 9 is a drawing showing the 1st example of unit switch S1-1 of operation in drawing 8. Drawing 9 is the same as that of the 1st unit switch S1-1 in the mentioned above example drawing 3 almost. Differences are the point that the number of incoming line became m from 8, and the point that the number of the outgoing lines became n from 2. It is determined to which outgoing line it outputs with reference to the address bit map table T-1 by header information x, y of the inputted cell.

[0075] Drawing 10 is a drawing showing the example of operation in the 2nd unit switch. The 2nd unit switch S2-1 has incoming line of m, it includes the outgoing line of n. n to incoming line 0- (n-1) is connected to the 1st outgoing line of unit switch S1-1 among incoming line of m. The outgoing line of n of 2nd unit switch S2-1 is connected to output port #0 - # (n-1), respectively. The address of the cell which reached the 2nd unit switch S2 like the mentioned above example is taken as just because it broke the incoming line number by the n outgoing line. Address queuing A2-0 corresponding to each outgoing line to A2 - (n-1) is provided. About operation of the MxN switch using the unit switch of mxn, as it is the same as that of the mentioned above example, explanation is omitted.

[0076] Example 3. The example which connects 3 steps of the 1st, 2nd unit switch, and constitutes the multistage connection part P from this example is explained. Drawing 11 is a line block diagram of the KxL switch at the time of using 3 steps of mxn unit switches. In a drawing, an input port is K. An output port is L. The feature of 3 stage constitution is using the 1st unit switch S1 for a further switch, and using the 2nd unit switch S2 altogether after the second step. Thus, what is necessary is to equip only the first step of 1st unit switch S1 with the address bit map table T. The second unit switch S2 used for the second step and a third stage judges the outgoing line from an incoming line number.

[0077] In a drawing, the portion of Q surrounding first step, the combination of the second step of unit switch is the same composition as the multistage connection part P of the 2 step connection shown on drawing 8. Thus, in the line concentrated type connection of 3 stage constitution, the switch group combined with the first step like the second step of Q becomes what gathered. The outgoing line n of the second step of 2nd unit switch is connected to a plurality of meetings and the incoming line m of the 2nd unit switch S2 of a third stage. As mentioned above, the multistage connection part P in the case of 3 stage constitution is constituted. The number of the multistage connection parts P is L/n. But, below the decimal point of L/n shall be revalued. As an output port different, respectively is assigned to each multistage connection part P, it can respond to the output port of L. The conventional example 1 describes and the difference from 3 step connection is a point with less number of the unit switches of a third stage than the second step with less number of the second step of unit switches than the first step. If this gives the address determining function of multiple address cells only to the 1st unit switch S1 used for the first step and there is necessity in it, it will copy a cell. And in the 2nd unit switch used next second step, it is the point that the address of a cell can be judged from an incoming line number. Thus, what is necessary

is to equip with the address bit map table T only the first unit switch S1 used in the first step. Although it is 3 stage constitution in drawing 11, it can also be made much more number of stages.
[0078] Next, the case of the number of the input port in the case of 3 stage constitution and output ports and 2 stage constitution is compared. The 1st, 2nd unit switch sets to m= 32 and n= 8, and is based on the case where it is referred to as M input / output port = N=128, using the 1st 4 unit switches S1. It is set to input/output port K = L =512, when this 2 stage constitution is extended and it is considered as 3 stage constitution. If it is generally i stage constitution, it will become number of input / output port =32 x 4(i-1) . Thus, the increase in an input port and an output port is easy by combining further the basic constitution by the line concentration shape connection of the 1st unit switch S1 and the 2nd unit switch S2. That is, it can extend easily, without spoiling a certain composition now.
[0079] This example described the case of multistage constitution as mentioned above focusing on the case where 3 steps of the 1st, 2nd unit switch is connected. It can respond to many input ports and an output port by using the 1st unit switch S1 for the first step, and using the 2nd unit switch S2 after the second step. It can extend easily to the increase in an input port and an output port, without spoiling the present composition.
[0080] Example 4. In this example, in order to identify the address of multiple address cells, one example which introduces a multiple address call number is described.
[0081] Drawing 12 is a line block diagram of the MxN switch by the line concentration shape connection in case an incoming line group unit defines a multiple address call number. In the drawing, multiple address identifier allocation means D has set the input port in the preceding paragraph which branches in the multistage connection part P. Multiple address identifier allocation means D gives a multiple address call number based on header information, when the inputted cells are multiple address cells. As other components are the same as that of what was explained by

the mentioned above example drawing 8, explanation is omitted. By the conventional example 1, the multiple address call number was introduced with the whole device, and reducing the amount of address bit map tables was shown. If this idea was applied to the line concentration shape connection as it was, the efficiency of the address bit map table T is bad. Next, as shown on drawing 12, a plurality of incoming lines which the 1st unit switch S1 accommodates is made into an incoming line group, and a multiple address call number is defined by making this into a unit. It is better for the utilization ratio of the address bit map table T to define a multiple address call number as an incoming line group unit in the 1st unit switch S1, rather than the whole device defines a multiple address call number as a specific input port is targeted.

[0082] The multiple address call number by multiple address identifier allocation means D is given to a cell as an extra header, as shown on drawing 13. Or as shown on drawing 14, it may give by another line.

[0083] Drawing 15 is a drawing showing the example of operation in the 1st unit switch S1-1. In the drawing, the cells inputted into input port #0 and # (m-2) are multiple address cells, and the extra header is given to the cell. The header processing circuit 131 investigates the extra header of the cell inputted into input port #0, and obtains the multiple address call number Y. The write buffer selection circuitry 111 judges with the outgoing line 1 and (n-1) being addresses with reference to the address bit map table T-1 with the multiple address call number Y. The multiple address cells inputted from input port # (m-2) get to know an address similarly based on the multiple address call number Z attached to the extra header. An extra header is excluded when outputting from the 1st unit switch S1. Or an extra header may be used in order to add other information.

[0084] This example described one example which introduces a multiple address call number as mentioned above. When inputting a multiple address call number, a plurality of input ports which the 1st unit switch S1 accommodates are made into an

incoming line group, and a multiple address call number is defined by making this into a unit. But, how to assign an incoming line group is good also considering the input port corresponding to a plurality of unit switches as 1 incoming line group. In this case, corresponding to the input port corresponding to a plurality of these unit switches, it has multiple address identifier allocation means D. The utilization ratio of an address bit map table becomes still better by dividing a plurality of input ports into an incoming line group as mentioned above, and introducing a multiple address call number to the incoming line group.

[0085] Example 5. This example describes the example which refers to the virtual path identifier / virtual channel identifier (VPI/VCI) value in a header as header information.

[0086] When carrying out the direct reference of the VPI/the VCI value in a header, multiple address identifier allocation means D of the mentioned above example becomes unnecessary, and the hardware scale of the whole device can be made small. The example of the address bit map table T at this time is shown on drawing 16. In the case of the conventional example 1, the direct reference of the VPI/the VCI value in a header cannot be carried out. Because, as VPI/VCI value is defined per incoming line, it is different incoming line and the value of the same VPI/VCI may be used. Thus, as it cannot judge in the cell which arrived from which incoming line if the second step switch and a third stage switch are only VPI/VCI in the conventional example 1, when judging the address bit map table T, it is because incoming line information must also be added. However, refer to the address bit map table T only for the 1st unit switch S1 in the data exchange device shown in the mentioned above example. The 1st unit switch S1 is connected to the input port. Thus, with reference to the address bit map table T, the outgoing line can be determined from VPI/VCI value, and an input port number by the 1st unit switch S1.

[0087] Example 6. This example measures the capacity of the address bit map table T about the case of 3 step connection of the conventional example 1, and the case of the line concentration shape connection explained in the mentioned above example. Thus, capacity is computed about each case and then both are compared.

[0088] The precondition for comparing is raised to drawing 17 and drawing 18. Drawing 17 is a precondition which becomes common. Drawing 18 is a parameter.

[0089] 1. Calculate the amount of address bit map tables in 3 step connection of the conventional example 1. Here, t2>=M is assumed as conditions which can perform 3 step connection.

(1) The 1st step of address bit map table capacity (the 1st step of address bit map table capacity)

= ct(line) x t(sequence) x (M/t)

=ctM(bits)

(2) The 2nd step of address bit map table capacity (the 2nd step of address bit map table capacity)

= cM(line) x t(sequence) x (M/t)

= cM^2 (bits)

(3) The 3rd step of address bit map table capacity (the 3rd step of address bit map table capacity)

= cM(line) x t(sequence) x (M/t)

= cM^2 (bits)

(4) With as mentioned above, the switch (sum total of the address bit map table capacity of all the switched networks) connected 3 steps

= c ($tM+2M^2$) (bits)

[0090] 2. In the amount line concentration type connection of address bit map tables in the line concentration shape connection, the following relations between the input port M of the whole switch, incoming line m of a unit switch, outgoing line n, and the number of stages k.

M<=m x (m/n)(k-1)

as stated previously, the 1st step of address bit map table capacity turns into the whole capacity.
(Sum total of the address bit map table capacity of all the switched networks)
= cm(line) x n(sequence) x (M/m) x (M/n)
= cM^2 (bits)
[0091] 3. In order to calculate comparison simply, the whole input port M, considers the case where it can divide among incoming line m and a unit switch t. When line concentration shape connection is made and a number of stages is set to k when a pyramid can be constructed exactly namely, the case where the relation $M=m \times (m/n)^{(k-1)}$
is materialized is examined. Drawing 19 is the drawing which compared the calculated value of the address bit map table. Here, in the case of $M=m \times (m/n)^{(k-1)}$, the ratio of both of the whole address bit map table R,
R= (line concentration shape connection / the conventional 3 step connection)
$= (cm^2(m/n)^{(2k-2)}) / (c\,(tm(m/n)^{(k-1)} + 2m^2(m/n)^{(2k-2)})) = 1/(t/m)\,((n/m)^{(k-1)}+2)$
Here, in the case of the line concentrated type switch, it is m>n although the relation to a problem of t, m, n becomes. In 3 step connection, it becomes a square switch, but when making an ATM switch generally, restrictions of the number of the outgoing lines can be considered from the I/O pin neck by the number of the number of incoming lines + outgoing lines, and the difficulty which builds queuing. Next, it is considered as m>=t>=n and fixed quantity evaluation is performed this time. Now when k>=2, m>n, m>=t>=n, the range of the range of R is 0<n/m<1, and it is shown on drawing 20 at the time of k= 2, on drawing 21 at the time of k= 3. However, it is not based on the value of t, n, m, c, but is set to 1/2>R>1/3. That is, the capacity of the address bit map table in the line concentration shape connection brings about the reduction effect becoming 1/3 to 1/2 compared with the conventional 3 step connection.

[0092] As mentioned above, this example examined the capacity of that address bit map table as compared with the conventional 3 step connection about the multiple address function in the concentrated type multistage constitution of lines. The same large scale switch is constituted and the case where the multiple address number of calls of the same number is realized around an input port is considered. It is not based on the size of a switch scale or a unit switch, but the total amount of address bit map tables brings about the reduction effect of being set to 1/3 - 1/2, in the line concentrated type multistage constitution as compared with the conventional 3 step connection.

[0093] Example 7. The mentioned above example described the case where the number of incoming lines of the 1st unit switch and the 2nd unit switch was the same. However, even when the numbers of incoming lines of the 1st unit switch and the 2nd unit switch differ, it is possible to constitute a large scale switch by line concentration shape connection described in the mentioned above example. For example, when using 3 1st unit switches of 32x8 for the 1st step, the 2nd unit switch of 24x8 is used for the 2nd step. When using 7 1st unit switches of 32x8 for the 1st step, the 2nd unit switch of 56x8 is used for the 2nd step. In both cases, as the number of the outgoing lines of the 1st unit switch and the 2nd unit switch is equal, the address of the cell in the 2nd unit switch determines an incoming line number by the remainder divided by the number of the outgoing lines. Or it may ask by other methods based on an incoming line number.

[0094] In a plurality of steps of line concentration shape connection, the 2nd unit switch with the number of incoming line different next 2nd step may be used.

[0095] Example 8. This example describes one example of the system which accommodates a plurality of low speed interfaces in the latter part of an output port.

[0096] Drawing 22 is a line block diagram of 16x32 switches by the 2 step connection corresponding to a low speed interface. By this example, in order to make it operate to common timing, the

example using common low speed interface identification timing is shown. The working speed of an ATM switch is 622 Mb/s, and low speed interfaces are 156 Mb/s. Input ports other than a low speed interface are the speed of 622 Mb/s. Though the low speed interface was connected to the input side, as it can treat as an input port of the speed of 622 Mb/s by a multiplex circuit, it is not necessary to consider whether a low speed interface exists in an input side. The number of input ports is 16 of #0 - #15. The number of output ports is 32 to #0-#31. 4 low speed interface #0-0 - #0-3 is connected to the point of output port #0 via the cell separation circuits 100. There are 16 multistage connection parts P-1 to P-16. In each multistage connection part P, concentrated type connection by 2 step connection of lines is made using the 1st 2 unit switches of 8x2, and the 2nd unit switch of 4x2. The 1st unit switch SL 1 is equipped with the address bit map table. The timing generating means 101 supplies low speed interface identification timing common to the 1st unit switch SL1 and 2nd unit switch SL2 and cell separation circuits 100. Address queuing equips the outgoing line 0 corresponding to the 1st unit switch SL 1, and the 2nd output port #0 of unit switch SL2 with 4 corresponding to each of 4 low speed interfaces. Although it is a case where the low speed interface is connected to output port #0, drawing 22 is the same even if the low speed interface is connected to which output ports other than output port #0.

[0097] Drawing 23 is the 1st block diagram of unit switch SL1 (low speed interface correspondence). The difference in the 1st unit switch S1 described as the 1st unit switch SL 1 corresponding to a low speed interface by drawing 2 is the following 2 points. Respectively corresponding to low speed interface #0-0 - #0-3, it has address queuing A1-00 - A1-03. It includes the selector 160 between the read out buffer selection circuitry 151, address queuing A1-00 - A1-03. The read out buffer selection circuitry 151 is sent to the storage control circuit 12 which determined the cell read from the buffer memory 11 with reference to the address queuing A1, and was matched with

the buffer memory 11 by making an applicable address into a read address. And switching of the cell readout circuitry 14 is controlled and it connects with the outgoing line which is going to output the buffer memory 11. Although the above is the same as the mentioned above read out buffer selection circuitry 19, the read out buffer selection circuitry 151 does not carry out the direct reference of address queuing A1-00 - A1-03 corresponding to a low speed interface, and it differs in that an address is obtained via the selector 160. Out of four address queuing A1-00 - A1-03 corresponding to a low speed interface, the selector 160 chooses one address queuing, reads the read address, and sends it to the buffer selection circuitry 151.

[0098] The timing chart of each outgoing line is shown on drawing 24. (イ) is low speed interface identification timing. (□) is the output timing of the cell in the outgoing line 0 of unit switch SL1-1 of drawing 22 1st is shown. In the outgoing line 0, when low speed interface identification timing is «High», the cell addressed to low speed interface #0-0 is outputted. Thus, the selector 160 certainly reads an address from address queuing A1-00 corresponding to low speed interface #0-0, when low speed interface identification timing is «High».

[0099] Drawing 25 is a drawing showing the 1st example of unit switch (low speed interface correspondence) SL1-1 of operation. The incoming line 0-7 is connected to input port #0 - 7 in the 1st unit switch SL1-1. The outgoing lines 0 and 1 are connected to the incoming line 0 and 1 of 2nd unit switch SL2-1. The outgoing line 0 leads to a low speed interface via the 2nd unit switch SL2-1. Low speed interface identification timing is supplied to the selector 160. As an address corresponding to header information, the address bit map table T-1 has low speed interface #0-0 - #0-3 and the outgoing line 1. Thus, by having the information corresponding to low speed interface #0-0 - #0-3 in the address bit map table T-1, it can be judged whether where of address queuing A1-00 - A1-03 should just make an address store.

[0100] Next, it explains to input port #1 taking the case of the case where multiple address cells b inputs into multiple address cells a and input port #5. However, explanation is omitted about the same operation as a conventional example. The write buffer selection circuitry 111 judges an address with reference to the address bit map table T-1 based on header information. It judges with the addresses of multiple address cells a being low speed interface #0-0, #0-1, and the outgoing line 1. The address exchange circuit 120 writes the address of the buffer memory 11 with which the cell a was stored to address queuing A1-00, A1-01, A1-1. Next, about multiple address cells b which reached input port #5, multiple address point and low speed interface #0-0, #0-2, #0-3, and the outgoing line 1 are similarly obtained from the address bit map T-1, and an address is written to address queuing A1-00, A1-02, A1-03, A1-1.

[0101] The operation at the time of outputting to the outgoing line is explained.

(1) The read out buffer selection circuitry 151 moves control to the selector 160. At this time, low speed interface identification timing considers it as «High». As low speed interface identification timing is «High», the selector 160 reads the address of the buffer memory 11 with which the cell a is stored from address queuing A1-00, and passes it to the read out buffer selection circuitry 151. The selector 160 sets the position of address queuing which should be read to the next by carrying out a counter +1, after reading an address from address queuing A1-00. The read out buffer selection circuitry 151 sends the received address to the storage control circuit 12, connects to the outgoing line 0 the buffer memory 11 which controls switching of the cell readout circuitry 14 and corresponds, and outputs the cell a.

(2) The read out buffer selection circuitry 151 reads the address of the cell a from address queuing A1-1, and sends it to the storage control circuit 12. The buffer memory which controls switching of the cell readout circuitry 14 and corresponds is connected to the outgoing line 1.

(3) The read out buffer selection circuitry 151 moves control to the selector 160. The selector 160 gets to know that address queuing read from the value of a counter to the next is address queuing A1-01, and reads the address of the cell a. The cell a addressed to low speed interface #0-1 is outputted to the outgoing line 0.
(4) The read out buffer selection circuitry 151 gets to know the address of the cell b from address queuing A1-1, and outputs the cell b to the outgoing line 1 similarly.
(5) The same operation is repeated and then the cell b addressed to low speed interface #0-2 is outputted to the outgoing line 0 at the outgoing line 0.
(6) As address is not stored by address queuing A1-1, output an idle cell to the outgoing line 1.
[0102] Thus, the cell addressed to low speed interface #0-0 - #0-3 is outputted to the outgoing line 0. As one in 4 address queuing A1-00 - A1-03 is chosen by the selector 160, the same cell addressed to a low speed interface drops to 1/4 of the number of cells outputted to the outgoing line 1. Thus, the cell abolition by buffer overflow in cell separation circuits can be lost.
[0103] Drawing 26 is the 2nd block diagram of unit switch SL2 (low speed interface correspondence). The difference between the 2nd unit switch SL 2 corresponding to a low speed interface and the 2nd unit switch S2 explained in the mentioned above example is the following 3 points. Corresponding to low speed interface #0-0 - #0-3, it has address queuing A2-00 - A2-03. The selector 160 reads with address queuing A2-00 - A2-03, and it has between the buffer selection circuitries 151. It includes the distribution circuit 170 between the address exchange circuit 120, address queuing A2-00 - A2-03.
[0104] The same low speed interface identification timing as the distribution circuit 170 and the thing supplied to the selector 160 at the 1st selector 160 of unit switch SL1 is supplied. The distribution circuit 170 distributes a cell to address queuing A2-00 - A-03 with reference to low speed interface identification

timing. The selector 160 sends out a cell like the 1st unit switch SL 1 by low speed interface identification timing. Drawing 24 (/\) shows the transmission timing of the cell in the outgoing line 0 of 2nd unit switch SL2-1. (□) and (/\), when low speed interface identification timing is «High», the cell addressed to low speed interface #0-0 is outputted. That is, the 1st step of outgoing line 0 (□) and the 2nd step of outgoing line 0 (/\) operate to the same timing.

[0105] Drawing 27 explains the example of operation in the 2nd unit switch (low speed interface correspondence) SL2-1. In the header processing circuit 132, header information is investigated and it is judged whether the cell which arrived is an idle cell. If it is not an idle cell, the write buffer selection circuitry 112 will be informed about an incoming line number. The write buffer selection circuitry 112 determines the outgoing line number of a cell by an incoming line number. The number of the outgoing line is searched for from the remainder which divided the incoming line number which the cell reached like the mentioned above example by the number of the outgoing lines of the 2nd unit switch. But, it may ask by other methods. The number of incoming line is 4, the 2nd unit switch SL2-1. Thus, the cell to which the incoming line 0 and the incoming line 2 reached the outgoing line 0 at the incoming line 1 and the incoming line 3 is outputted to the outgoing line 1. The cell a, a, b, b, b reach the incoming line 0. The cells a, b reach the incoming line 1. The cell e, f, g, g, g reach the incoming line 2. The cell f, g, h, i, j reach the incoming line 3. The address of the cells a, e which reached the incoming line 0 and the incoming line 2 distributes by the address exchange circuit 120, and is passed to the circuit 170. At this time, low speed interface identification timing considers it as «High». The distribution circuit 170 writes the address of the cells a, e in address queuing A2-00 from low speed interface identification timing being «High». And a counter is carried out

+1 and the position of address queuing which should be written in the next is set.

[0106] An address is written in the cell a and the cell f which reached the incoming line 1 and the incoming line 3 by the address exchange circuit 120 address queuing A2-1. Next, the cells a, f which reached the incoming line 0 and the incoming line 2 are distributed via the address exchange circuit 120, and an address is passed to the circuit 170. In the distribution circuit 170, the address of the cell a and the cell f is written in address queuing A2-01 by investigating a counter. Thus, the address is written to the address queuing A2. As the number of incoming line is 4, it distributes, and the circuit 170 writes 2 addresses of a cell at a time in 1 address queuing A2 at once. It will distribute, if 8 incoming line becomes, and the circuit 170 writes the address of 4 cells in the one address queuing A2 at once. As the distribution circuit 170 moves by one twice (the number of the number of incoming line / outgoing lines) the speed of a time slot, the distribution circuit 170 does not need a buffer.

[0107] At the same time as the address exchange circuit 120 notifies an address to the distribution circuit 170, it can write an address in address queuing A2-1. Or it may carry out by turns. Work of the selector 160 in the 2nd unit switch SL2-1 is the same as that of what was explained in the 1 st unit switch SL1-1.

[0108] As for address queuing A2-00 corresponding to a low speed interface - A2-03, an address is written by the distribution circuit 170 with reference to low speed interface identification timing. Thus, the address of the cell currently written to the 1st address queuing A1-00 of unit switch SL1 is written to address queuing A2-00 corresponding to the same low speed interface #0-0 also in the 2nd unit switch SL2-1. Thus, by supplying low speed interface identification timing to all the unit switches, distributing with the selector 160, and referring to it in the circuit 170, the cell stored by address queuing with the 1st unit switch is stored by address queuing corresponding to the same low speed interface of the 2nd unit switch. The selector 160 in the 2nd unit

switch SL 2 chooses address queuing in order by low speed interface identification timing. Thus, a cell can be outputted to low speed interface #0-0 - #0-3 corresponding to address of cell. Compared with the output from queuing corresponding to the usual outgoing line, the number of times of the data outputted from a plurality of queuing stored for every low speed interface has decreased by equipping the 1st, 2nd unit switch with a selector. Thus, the cell abolition by buffer overflow in separation circuits can be lost. Also in the cell separation circuits 100, as shown on drawing 24 (二) - (ト), the cell is sent out to each low speed interface #0-0 - #0-3 by low speed interface identification timing.

[0109] Thus, address queuing corresponding to a low speed interface is given to the 1st unit switch and 2nd unit switch, by giving the same low speed interface identification timing as a selector, a distribution circuit, and cell separation circuits, even if it makes the 1st, 2nd unit switch into multistage constitution, a cell can be sent out to a desired low speed interface. The same may be the mentioned above of the case of a plurality of steps of composition.

[0110] This example described the low speed interface as mentioned above about the cell exchange device connectable with an input port or an output port. This cell exchange device consists of a plurality of 1st, 2nd unit switches. The 1st unit switch performs the copy and address distribution of a cell. The 1st, 2nd unit switch operates synchronizing with low speed interface identification timing. As the 2nd unit switch judges destination outgoing lines, namely, an address low speed interface, to the inputted cell by the incoming line number and low speed interface identification timing, in the 2nd unit switch, the address bit map table of multiple address cells is unnecessary. The cell exchange device to which large scale exchange is made is obtained by connecting such 1st, 2nd unit switch to a plurality of step line concentration type. When a cell exchange device performs exchange for a plurality of cells inputted from the multiple input

port and the mentioned above cell is outputted to an output port, the cell abolition by buffer overflow in cell separation circuits can be lost. Thus, when outputting a cell to cell separation circuits from an ATM switch, it can avoid exceeding the capacity of each low speed interface. By what a time change of cell arrival is absorbed for by the buffer memory of the 1st, 2nd unit switch. The buffer memory in the 1st, 2nd unit switch was shared and used between each low speed interface, the buffer utilization ratio was raised, and low waste ratio realization was achieved in the small total amount of buffers by the whole system.

[0111] Example 9. Drawing 28 is a line block diagram of the MxN switch which used the 1st, 2nd unit switch (mxn) corresponding to a low speed interface. The cell exchange device of arbitrary scales can be built using the 1st, 2nd unit switch corresponding to the same low speed interface as the mentioned above example. The number of low speed interfaces is arbitrary. There may be how many output ports that lead to a low speed interface not only in output port i.

[0112] Example 10. This example describes one example of the system which accommodates a high speed interface.

[0113] Drawing 29 is a line block diagram corresponding to a high speed interface. The drawing has represented only the multistage connection part P-1. One high speed interface is connected to the latter part of output port #0 - #4 by the cell multiplex circuit 180. 2 steps of the 1st, 2nd unit switch are connected for large scaling. The 1st unit switch SH1- 1, the 2nd unit switch SH2-1, SH1-2 both have 16 incoming lines and 8 outgoing lines. The feature of the 1st, 2nd unit switch is having one address queuing to a plurality of outgoing lines corresponding to a high speed interface. Considering the case where the high speed interface is connected to the input port side by cell separation circuits, it is necessary to save the arrival order foreword of a cell. Thus, when a cell arrives simultaneously in the 1st, 2nd unit switch, a cell shall be processed in order of the incoming line 15 from the incoming line 0.

[0114] Drawing 30 is the 1st block diagram of unit switch (high speed interface correspondence) SH1. The 1st feature of unit switch (high speed interface correspondence) SH1 is a point which has 1 address queuing A1-H to a plurality of outgoing lines. A plurality of outgoing lines is the outgoing lines corresponding to the output port connected to a high speed interface by the cell multiplex circuit 180. It reads with address queuing A1-H, and has the distribution circuit 190 between the buffer selection circuitries 152. The distribution circuit 190 reads an address to 1 time of applicable a plurality of outgoing lines of every several sequentially from the head of the address stored by address queuing A1-H. The address read by the distribution circuit 190 is passed to the read out buffer selection circuitry 152.
[0115] Drawing 31 is the 2nd block diagram of unit switch (high speed interface correspondence) SH2. It has a plurality of address queuing A2-H corresponding to the outgoing line, and has the distribution circuit 190. Work of address queuing A2-H and the distribution circuit 190 is the same as that of drawing 30.
[0116] Operation of the 1st step of 1st unit switch is explained using drawing 32. In a drawing, «イ» - «チ» express a cell, and a flow after being inputted into queuing until it is outputted is shown. In 1st unit switch SH 1, 1 address queuing A1-H is given to 4 outgoing lines 0-3 corresponding to a high speed interface. In 1st unit switch SH1-1, the cell is located in a line in order of «イ», «口», «ノ\», «二» from the head in address queuing A1-H which accommodates a high speed interface. A high speed interface may be connected to four input ports via cell separation circuits. Thus, as the order relation of the cell on the high speed interface of an output destination change is saved, 4 addresses of «イ», «口», «ノ\», «二» are read from address queuing A1-H at once by the separation circuits 190. The cell with which address of «イ», «口», «ノ\», «二» was passed to read out buffer selection circuitry 152, and read out buffer selection circuitry 152 was

stored by buffer memory 11, «イ» as the outgoing line 0, «口» as the outgoing line 1, «ハ» as the outgoing line 2 and «二» as the outgoing line 3. About 4 cells sent out simultaneously, preliminary, the outgoing line 0 top uses a four outgoing lines top as the cell sent out previously in time, and makes it order with the order of the outgoing lines 1, 2, 3 below. The cell of 1st unit switch SH1-2 is the same also about «ホ» - «チ».

[0117] The 2nd operation of unit switch SH2 is explained using drawing 33. The 2nd unit switch SH 2 is provided with 1 address queuing A2-H to 4 outgoing lines 0-3 corresponding to a high speed interface. The 2nd unit switch SH2-1 is provided with 16 incoming lines, and it determines the outgoing line from an incoming line number. The write buffer selection circuitry 112 makes remainder which divided the incoming line number of the cell which arrived like the mentioned above example by the number of the outgoing lines the destination outgoing lines number. However, other methods may be used. As the outgoing lines 0-3 correspond to address queuing A2-H if remainder which divided the incoming line number by the number of the outgoing lines is made into destination outgoing lines, the cell which reached the incoming line 0, 1, 2, 3, 8, 9, 10, 11 will be written in. The address exchange circuit 120 receives an address from the write buffer selection circuitry 112, and when addresses are the outgoing lines 0-3, it writes it in address queuing A2-H. When an address is 4, it writes in address queuing A2-4. ...when an address is 7, it writes in address queuing A2-7.

[0118] Here, the order inversion of the cell between the incoming line 0, 1, 2, 3 and between the incoming line 8, 9, 10, 11 must be made indispensable. Thus, the address exchange circuit 120 writes an address in young incoming line numerical order, namely, the small order of an address, at address queuing A2-H. The turn of the cell written in address queuing becomes the order of cell «イ», «口», «ハ», «二», «ホ», «ヘ», «ト», «チ».

However, as the order inversion of the cell between the incoming line 0, 1, 2, 3 and between the incoming line 8, 9, 10, 11 does not take place even if it becomes «イ», «ホ», «口», «ヘ», «ノ\», «ト», «二», «チ», for example, it is possible. The address of cell «イ», «口», «ノ\», from address queuing A2-H is read at once by the distribution circuit 190, and is passed to the read out buffer selection circuitry 152. The read out buffer selection circuitry 152 passed the cell from the buffer memory 11, «イ» as the outgoing line 0, «口» as the outgoing line 1, ... «二» as the outgoing line 3. Same processing is performed also about cell «ホ», «ヘ», «ト», «チ». And cell is transmitted in order of «イ», «口»... «チ» to a high speed interface by the latter cell multiplex circuit 180. It is also the same as when connecting the 1st, 2nd a plurality of steps of unit switch.

[0119] This example described the high speed interface as mentioned above about the cell exchange device connectable with an input port or an output port. This cell exchange device consists of a plurality of 1st, 2nd unit switches. The 1st unit switch performs the copy of a cell, and distribution of an address. The 2nd unit switch judges destination outgoing lines from the incoming line number to the cell which arrived. The order relation defined preliminary is saved at a plurality of incoming lines corresponding to a high speed interface, and an arrival cell is written in one queuing. The cell exchange device to which large scale exchange is made is obtained such by connecting the 1st, 2nd unit switch to a plurality of steps of line concentration type. When performing exchange for a plurality of cells inputted from a plurality of incoming lines in the 1st, 2nd unit switch and outputting the mentioned above cell to the outgoing line, a priority is given and processed fixed to a plurality of incoming lines and the outgoing line, and an order of a cell of having

arrived simultaneously is saved. It became possible to accommodate a high speed interface by managing the outgoing plurality of these lines by one queuing.

[0120] Example 11. Drawing 34 is a line block diagram of 128x32 switches at the time of using the incoming line 32 and the outgoing line 8 for the 1st unit switch S1, and using the incoming line 16 and the outgoing line 4 for the 2nd unit switch S2. In the mentioned above example, in order to realize 128x8 in the multistage connection part P, 32x8 was used for the 2nd unit switch S2. But, the same function is realizable even if it uses 2 16x4 for the 2nd unit switch S2, as shown on a drawing. In this case, the outgoing lines 0-3 of all 1st unit switch S1-1 - S1-4 are connected to the 2nd unit switch S2-1. The outgoing lines 4-7 of all 1st unit switch S1-1 - S1-4 are connected to the 2nd unit switch S2-2. Thus, the number of incoming lines of the 1st unit switch S1 and the 2nd unit switch S2 may differ from the number of the outgoing lines. The same of the 1st, 2nd unit switch may be the mentioned above of the case corresponding to low speed interface and a high speed interface correspondence.

[0121] Example 12. The case where an address bit map table is shared is explained using drawing 35. The 1st unit switches S1-1, S1-2 share and use the address bit map table T-1. The 1st unit switches S1-3, S1-4 share the address bit map table T-2. Thus, an address bit map table can be shared and used among a plurality of 1st unit switches. Or all 1st unit switches may share one address bit map table. The same of the 1st, 2nd unit switch may be said about the case corresponding to low speed interface and a high speed interface correspondence.

[0122] Example 13. In the example, although the ATM switch into which a cell is inputted was described, if multiple address cells are used as multiple address data, the same switch can be provided also to the data exchange device used for general data communications.

[0123]

[Effect of the invention] According to the 1st invention, the number of input ports connectable with a data exchange device can be increased by carrying out multistage constitution of a plurality of unit switches with few incoming lines and the numbers of the outgoing lines.

[0124] According to the 2nd invention, the number of output ports connectable with a data exchange device can be increased.

[0125] According to the 3rd invention, the 1st unit switch can know the outgoing line which should output multiple address data on a table. The output destination change of each multiple address data is easily replaceable by exchange of a table.

[0126] According to the 4th invention, the 2nd unit switch has an unnecessary table for getting to know the address of the inputted data. Thus, the quantity of the table which it has as a data exchange device is reducible.

[0127] According to the 5th invention, a cell is exchangeable by the virtual path identifier and virtual channel identifier of a cell.

[0128] According to the 6th invention, the size of the table which determines an address can be made small and an address can be searched efficiently. As the size of a table is small, RAM can be made to be able to store a table and it can build in the 1st unit switch. As it divides and has a table, change of a table is easy.

[0129] According to the 7th invention, a plurality of unit switches can share 1 table, thus, batch management is possible.

[0130] According to the 8th invention, a multiple address identifier can determine the outgoing line. As a multiple address identifier is used, the size of a table can be made small.

[0131] According to the 9th invention, what is necessary is just to define a multiple address identifier for some input ports, thus, assignment of a multiple address identifier becomes easy.

[0132] According to the 10th invention, also when a low speed interface is accommodated, it can be applied.

[0133] According to the 11th invention, the data addressed to each low speed interface can be certainly outputted to the low speed interface of an address, and, also, the cell abolition by

buffer overflow in separation circuits can be lost. A time change of arrival of a cell is absorbable by the 1st, 2nd unit switch.
[0134] According to the 12th invention, also when a high speed interface is accommodated, it can be applied.
[0135] According to the 13th invention, the order relation of data can be saved and it can output to the high speed interface by the side of an output port.

[Brief description of the drawings]
[Drawing 1] is the line block diagram of 32x32 switches by 2 step connection.
[Drawing 2] is the block diagram of the 1st unit switch.
[Drawing 3] is the drawing showing the example of operation in the 1st unit switch S1-1.
[Drawing 4] is the drawing showing the example of operation in the 1st unit switch S1-3.
[Drawing 5] is the drawing showing the example of operation in the 1st unit switch S1-63.
[Drawing 6] is the block diagram of the 2nd unit switch.
[Drawing 7] is the drawing showing the example of operation in the 2nd unit switch.
[Drawing 8] is the line block diagram of the MxN switch by 2 step connection.
[Drawing 9] is the drawing showing the example of operation in the 1st unit switch S1-1 of a MxN switch.
[Drawing 10] is the drawing showing the example of operation in the 2nd unit switch S2-1 of a MxN switch.
[Drawing 11] is the line block diagram of the KxL switch by the line concentration shape connection at the time of using 3 steps of unit switches of mxn.
[Drawing 12] is the line block diagram of the MxN switch by the line concentration shape connection when an incoming line group unit defines a multiple address item number.
[Drawing 13] is the drawing showing the example which gives a multiple address item number to an extra header.

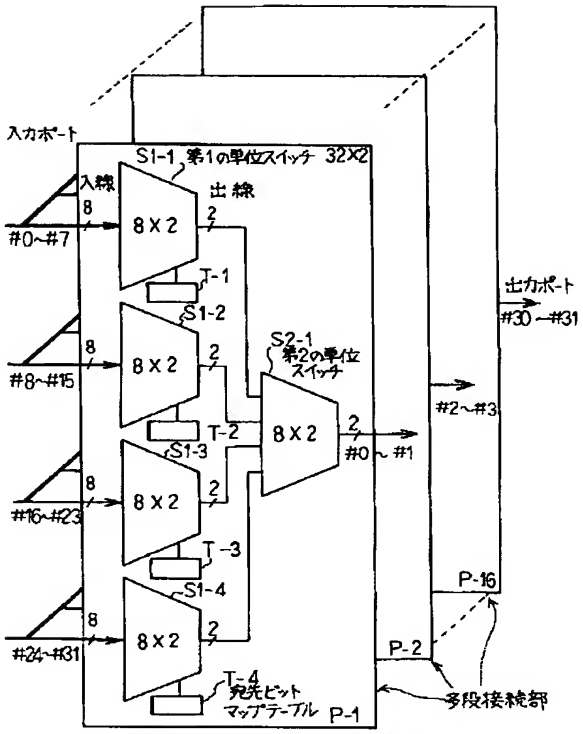
[Drawing 14] is the drawing showing the example which gives a multiple address item number to a switch by another line.
[Drawing 15] is the drawing showing the example of operation in the 1st unit switch at the time of using a multiple address item number.
[Drawing 16] is the drawing showing the example of the address bit map table in the case of referring to direct VPI and VCI value for every input port.
[Drawing 17] is the drawing showing the common item for comparison.
[Drawing 18] is the drawing showing each parameter.
[Drawing 19] is the drawing which measured the quantity of the address bit map table.
[Drawing 20] is the drawing showing the range of the ratio R of the capacity of an address bit map table (k = 2).
[Drawing 21] is the drawing showing the range of the ratio R of the capacity of an address bit map table (K = 3).
[Drawing 22] is the line block diagram of the line concentration shape connection corresponding to a low speed interface.
[Drawing 23] is the block diagram of the 1st unit switch (low speed interface correspondence).
[Drawing 24] is the drawing showing the timing chart of each outgoing line.
[Drawing 25] is the drawing showing the 1st example of unit switch SL1-1 of operation.
[Drawing 26] is the block diagram of the 2nd unit switch (low speed interface correspondence).
[Drawing 27] is the drawing showing the example of the 2nd unit switch SL2-1 of operation.
[Drawing 28] is the line block diagram of the MxN switch corresponding to a low speed interface.
[Drawing 29] is the line block diagram of the line concentration shape connection corresponding to a high speed interface.
[Drawing 30] is the block diagram of the 1st unit switch (high speed interface correspondence).

[Drawing 31] is the block diagram of the 2nd unit switch (high speed interface correspondence).
[Drawing 32] is the drawing showing the example of the 1st unit switch (high speed interface correspondence) of operation.
[Drawing 33] is the drawing showing the example of the 2nd unit switch (high speed interface correspondence) of operation.
[Drawing 34] is the line block diagram of the line concentration shape connection constituted from the 1st unit switch and the 2nd unit switch with the different number of incoming line, and the number of the outgoing lines.
[Drawing 35] is the line block diagram of the line concentration shape connection in the case of sharing an address bit map table.
[Drawing 36] is the drawing showing the speech path composition model in the conventional example 1.
[Drawing 37] is the route information table capacity comparison drawing in the conventional example 1.
[Drawing 38] is the line block diagram of the header processing part in the conventional example 1.
[Drawing 39] is the drawing showing large scaling by the pyramid composition in the conventional example 2.
[Drawing 40] is the block diagram showing the whole cell exchange device in the conventional example 3.
[Drawing 41] is the block diagram of the ATM switch in the conventional example 3.
[Drawing 42] is the drawing showing the example of an internal circuit of the cell multiplex circuit in the conventional example 3.
[Drawing 43] is the timing diagram of each part in the conventional example 3.
[Drawing 44] is the drawing showing the example of an internal circuit of the cell separation circuits in the conventional example 3.
[Drawing 45] is the timing diagram of each part in the conventional example 3.
[Drawing 46] is the drawing showing an example of address queuing in the ATM switch in the conventional example 3.

[Drawing 47] is the timing diagram of the outgoing line in the conventional example 3.
[Drawing 48] is the drawing showing the circuit accommodation method in the conventional example 4.

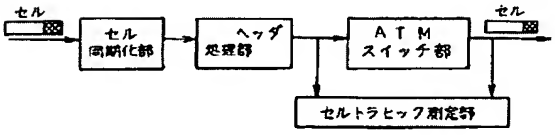
[Description of numerals]
1 An incoming line, 2 An outgoing line, 3 ATM switch, 4 A cell multiplex circuit, 5 A cell separation circuit, 6 An input port, 7 An output port, 8 A cell exchange device, 10 A header processing circuit, 11 A buffer memory, 12 A storage control circuit, 13 A cell circuit writing, 14 A cell readout circuitry, 15 A buffer control circuit, 16 A write buffer selection circuitry, 17 An address exchange circuit, 18 Address queuing, 19 A read out buffer selection circuitry, 21, 23 A cell speed adjustment buffer, 22 An address filter, 100 A cell separation circuit, 101 A timing generating means, 105 A multiple address processing means, 111, 112 A write buffer selection circuitry, 120 An address exchange circuit, 131, 132 A header processing circuit, 151, 152 A read out buffer selection circuitry, 160 A selector, 170 A distribution circuit, 180 A cell multiplex circuit, 190 A distribution circuit, S1-1, S1-2, S1-3, S1-4, S1-63, S1-M/m, S1 The 1st unit switch, T-1, T-2, T-3, T-4, T-M/m, T An address bit map table, S2-1, S2 The 2nd unit switch, P-1, P-2, P-16, P-N/n, P-L/n multistage connection part, A1-0, A1-1, A1-2, A2-0, A2-1, A2-2, A2- (n-1), A1-00, A1-01, A1-02, A1-03, A2-00, A2-01, A2-02, A2-03, A1-H, A2-H An address queuing, D-1, D-2, D-M/m Multiple address identifier allocation means, SL1-1, SL1-2, SL1-M/m The 1st unit switch (low speed interface correspondence), SL2-1 2nd unit switch (low speed interface correspondence), SH1-1, SH1-2 The 1st unit switch (high speed interface correspondence), SH2-1 The 2nd unit switch (high speed interface correspondence)

Drawing 1



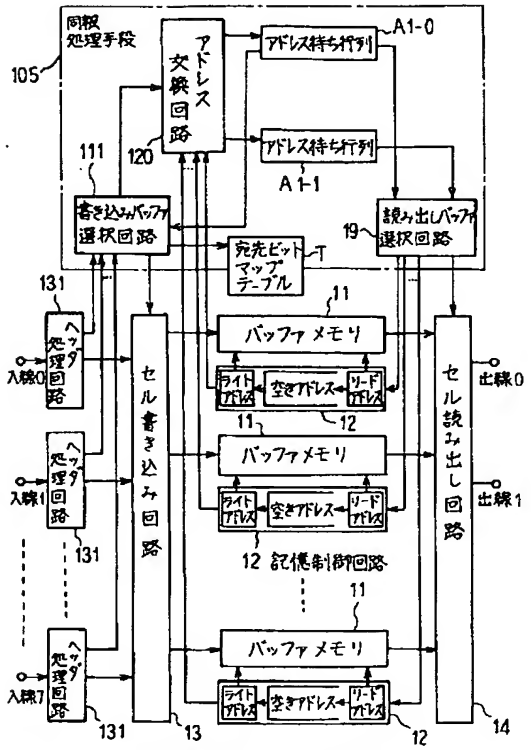
2段接続による32X32スイッチの構成図
（8X2の単位スイッチを用いた場合）

Drawing 36



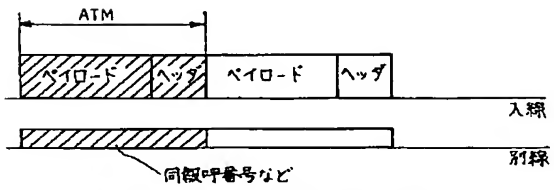
通話路構成モデル

Drawing 2



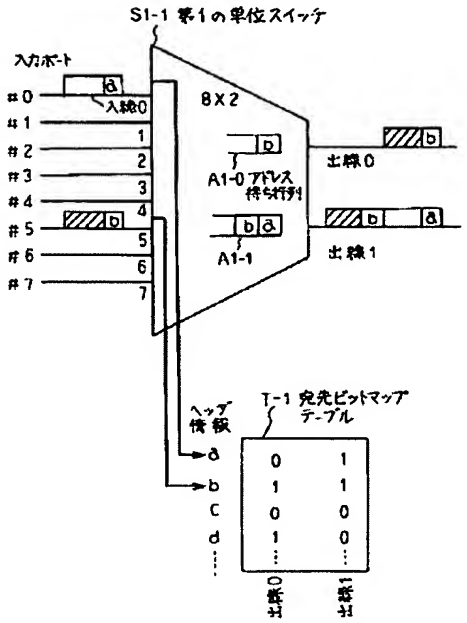
第1の単位スイッチブロック図

Drawing 14



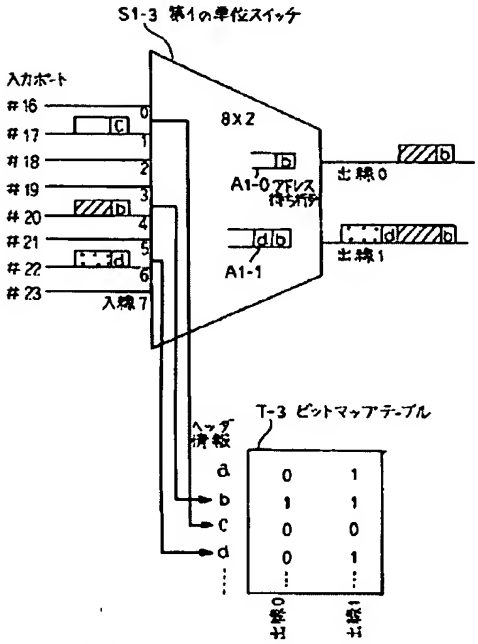
同報呼番号を別線でスイッチに付与する例

Drawing 3



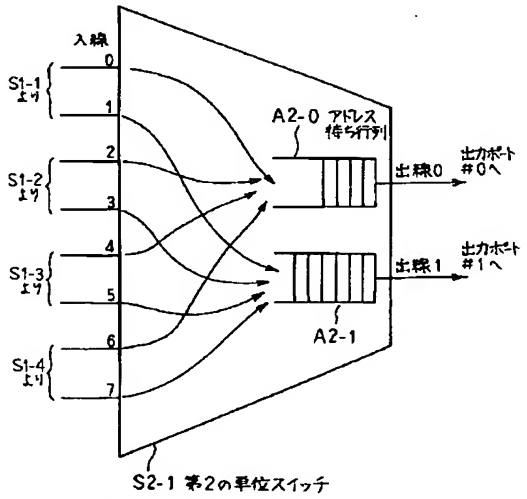
第1の単位スイッチS1-1における動作例

Drawing 4



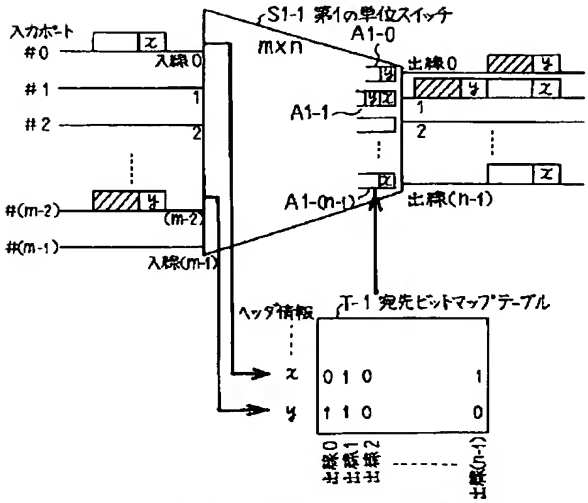
第1の単位スイッチS1-3における動作例

Drawing 7



第2の単位スイッチにおける動作例

Drawing 9



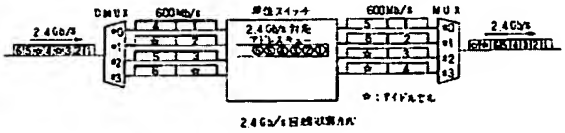
第1の単位スイッチS1-1における動作例

Drawing 17

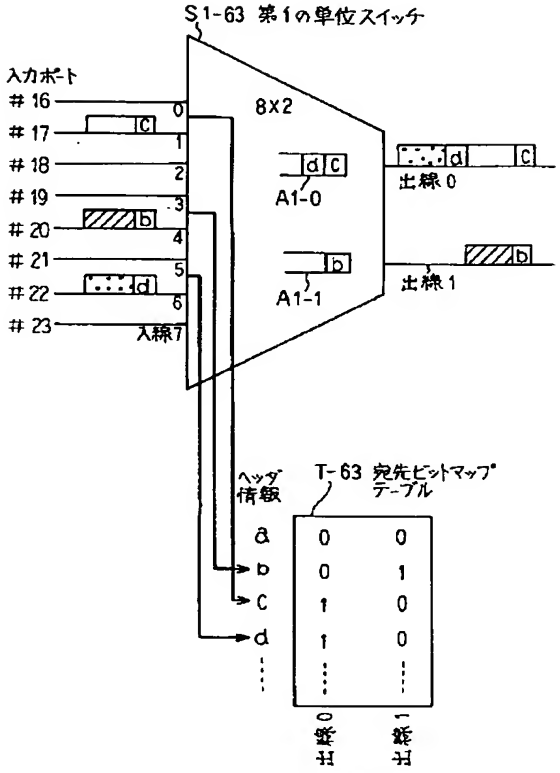
比較のための共通項目

共通となる前提条件			
番号	項 目	三段接続	集線形接続
1	システム全体で実現する規模	M×M	M×M
2	入力ポートあたりの同報呼の数	C本	C本

Drawing 48

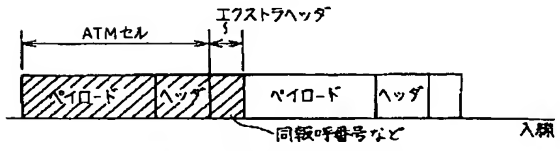


Drawing 5



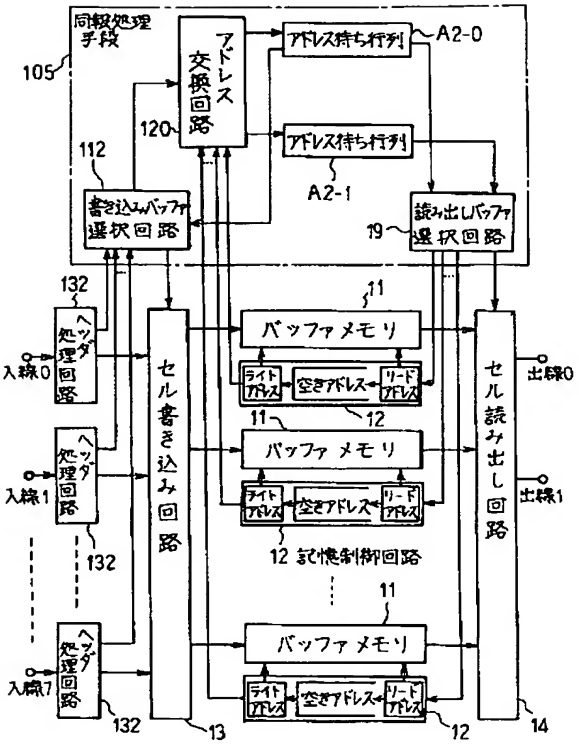
第1の単位スイッチS1-63における動作例

Drawing 13



同報呼番号をエクストラヘッダに付与する例

Drawing 6



第2の単位スイッチブロック図

Drawing 19

番号	条件	三段接続	単段形接続
1	全体の入線数をMとしたときの宛先ビットマップテーブルの量（一般解）	$C(tM+2M^2)$(bits)	CM^2(bits)
2	特に、$M = m \times (m/n)^{(K-1)}$ という関係が成立する場合の容量	$C\{tm(m/n)^{(K-1)} + 2m^2(m/n)^{(2K-2)}\}$	$Cm^2(m/n)^{(2K-2)}$
3	例えば、m=32, n=8, K=2, t=32, C=1K本, (すなわちM=128)の時の容量（具体例）	36 M (bits)	16 M (bits)

（Kは提案する集積形接続における段数を示すパラメータ）

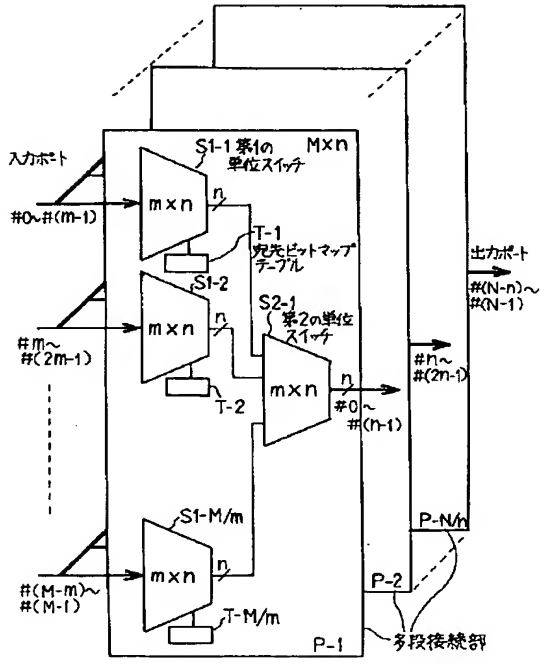
宛先ビットマップテーブルの量の比較

Drawing 18

各々のパラメータ

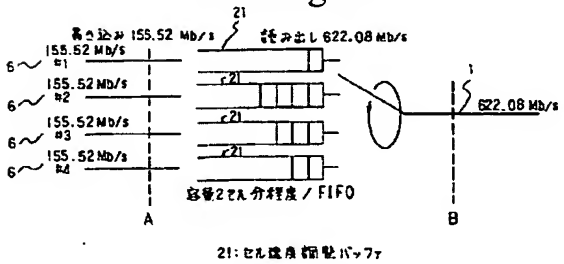
番号	項 目	三段接続	集積形接続
1	多段段数	3段 （固定）	K段
2	単位スイッチの規模	txt	mxn (m>nとする)

Drawing 8



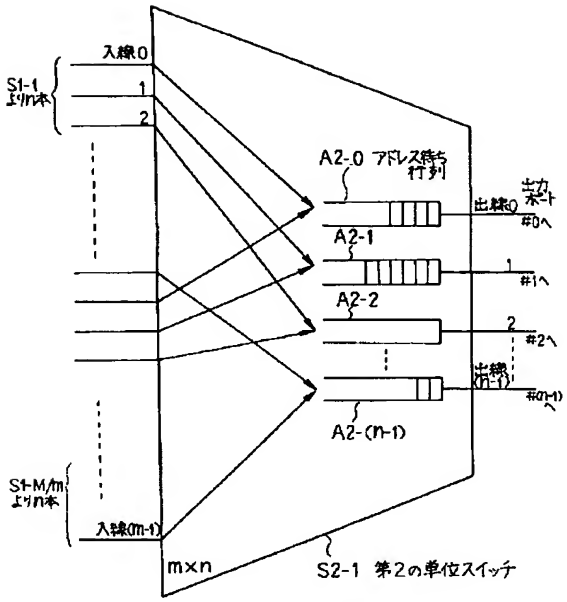
2段接続によるM×Nスイッチの構成図
(m×nの単位スイッチを用いた場合)

Drawing 42



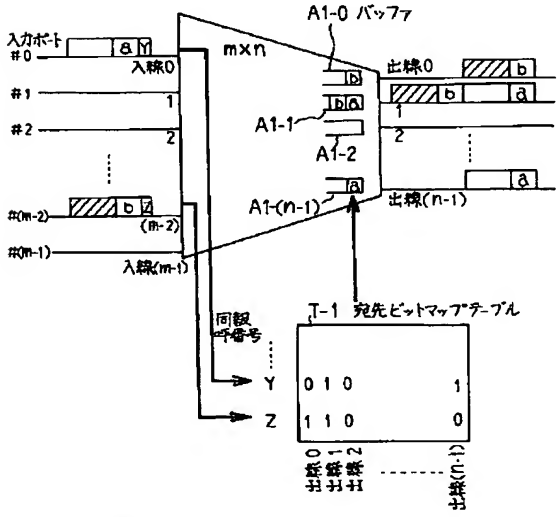
21: セル廃棄緩衝バッファ

Drawing 10



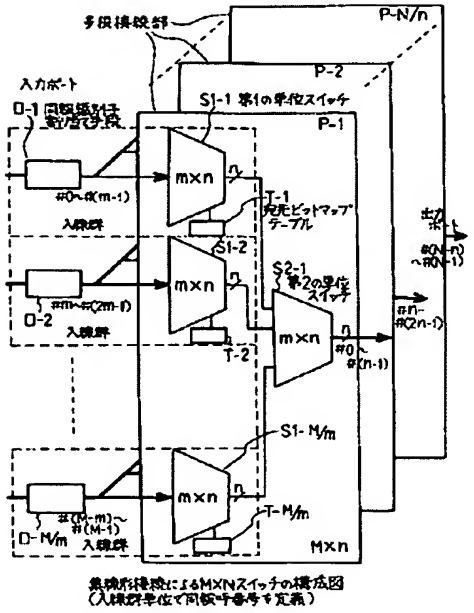
第2の単位スイッチにおける動作例

Drawing 15

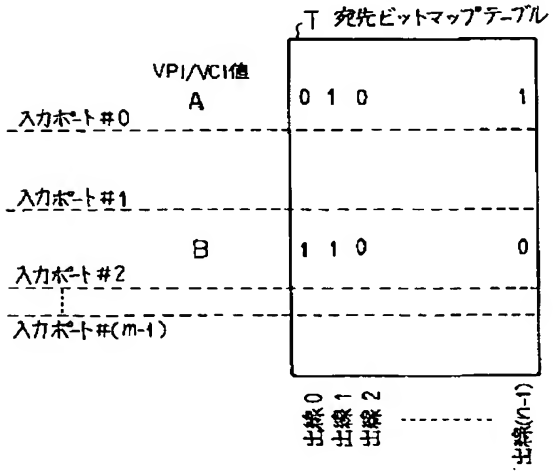


第1の単位スイッチS1-1における動作例

Drawing 12

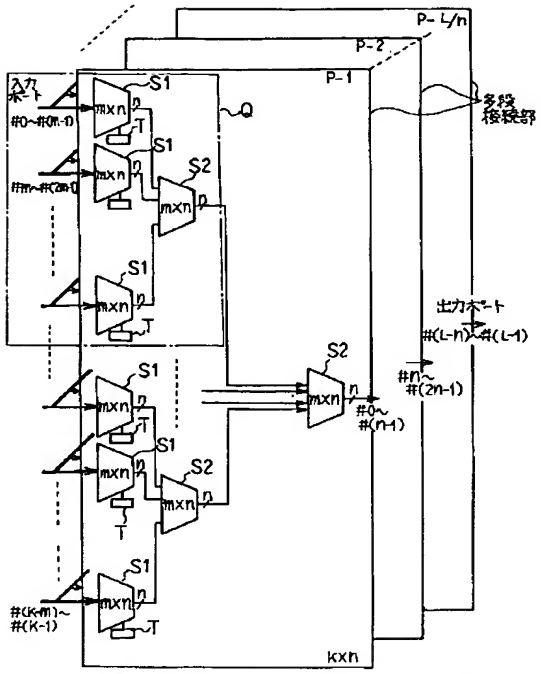


Drawing 16



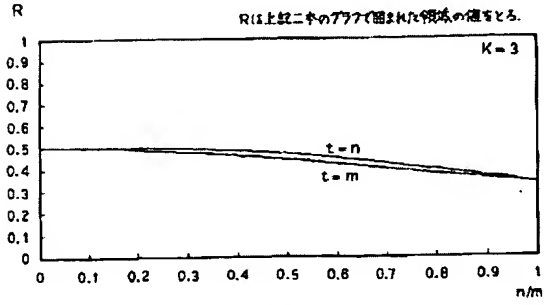
入力ポート毎に直接VPI/VCI値を参照する場合の
宛先ビットマップテーブルの例

Drawing 11



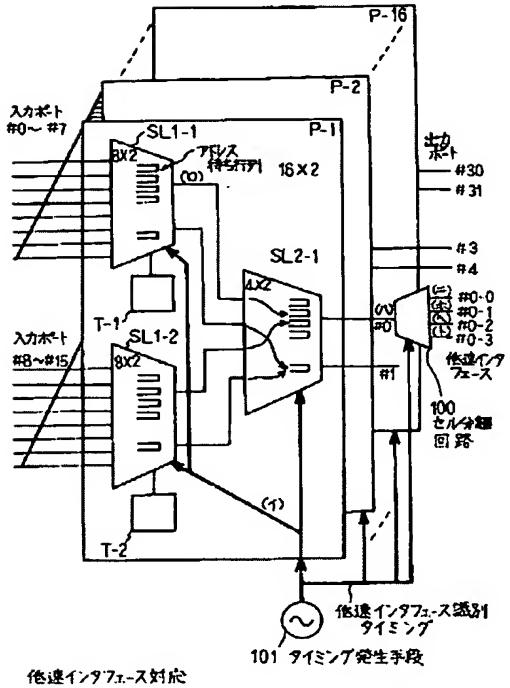
集線形接続によるK×Lスイッチの構成図(3段構成)
(m×nの単位スイッチを3段用いた場合)

Drawing 21



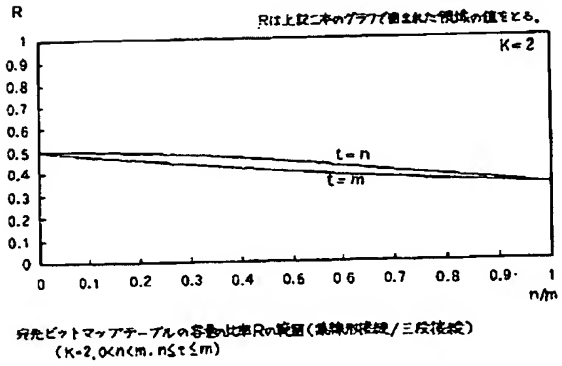
完全ビットマップテーブルの容量の比率Rの表図(集線形3段接続/三段接続)
(K=3, 0<n<m, n≦t≦m)

Drawing 22

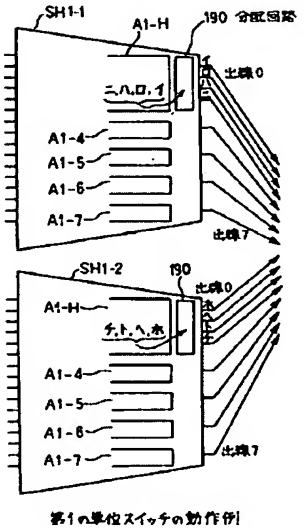


低速インタフェース対応

Drawing 20

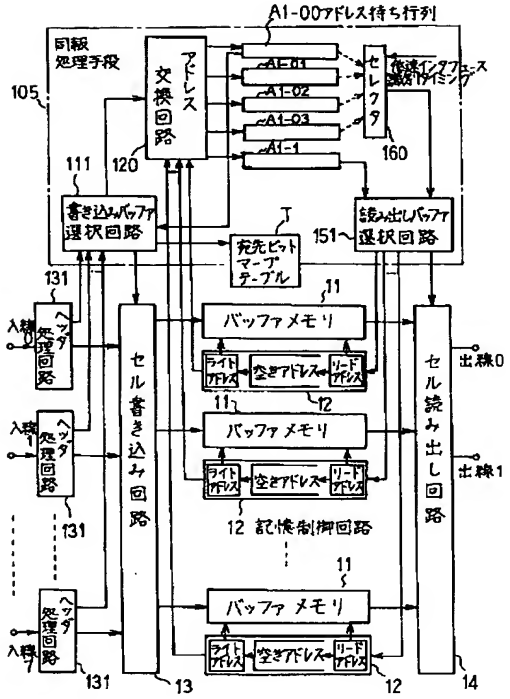


Drawing 32



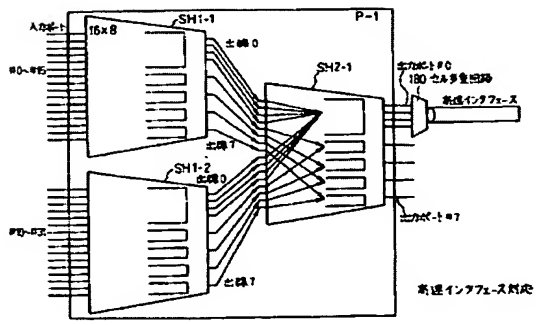
第1の単位スイッチの動作例

Drawing 23

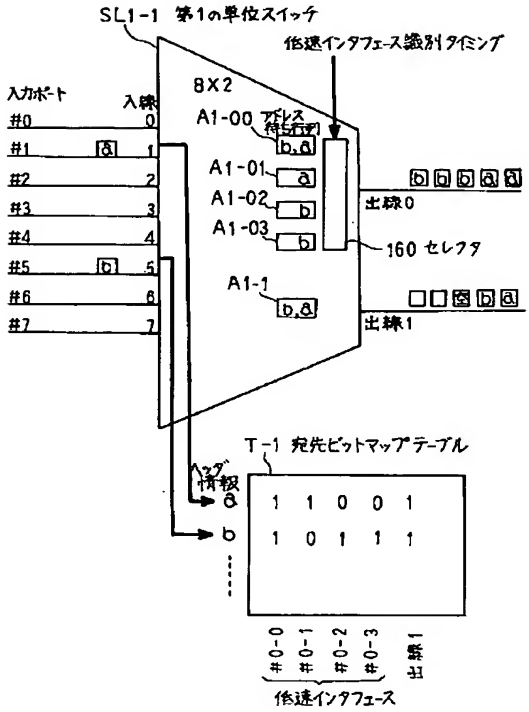


第1の単位スイッチ(低速インタフェース対応)

Drawing 29

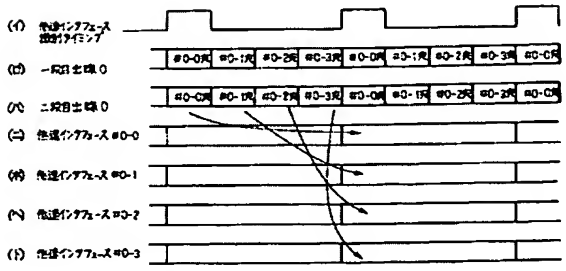


Drawing 25



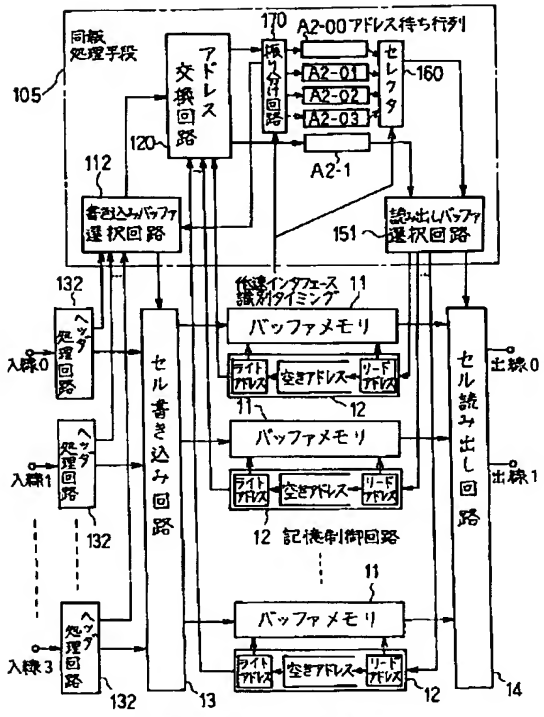
第1の単位スイッチ(低速インタフェース対応)SL1-1

Drawing 24



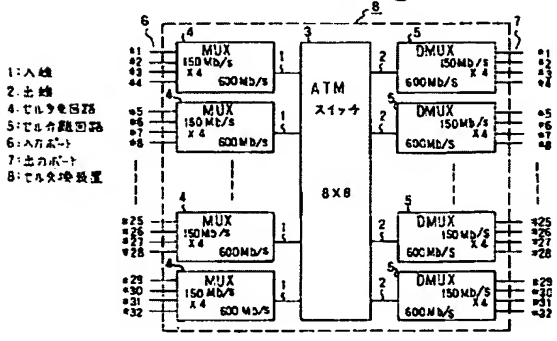
各出線のタイミングチャート

Drawing 26

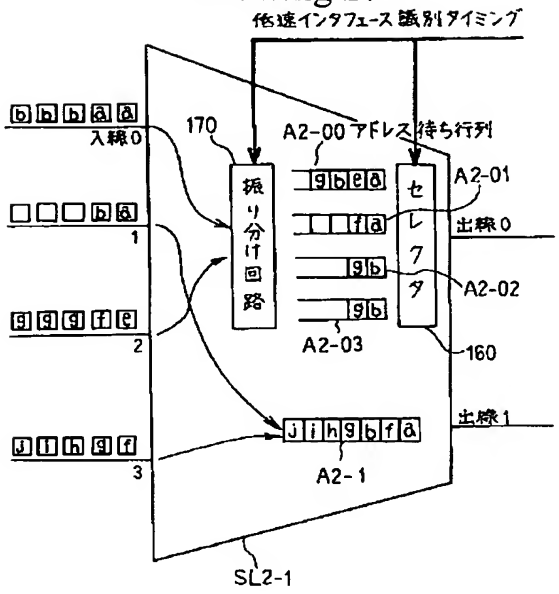


第2の単位スイッチ（他速インタフェース対応）

Drawing 40

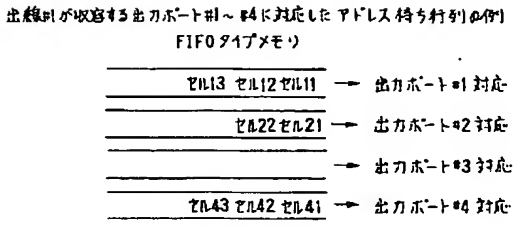


Drawing 27

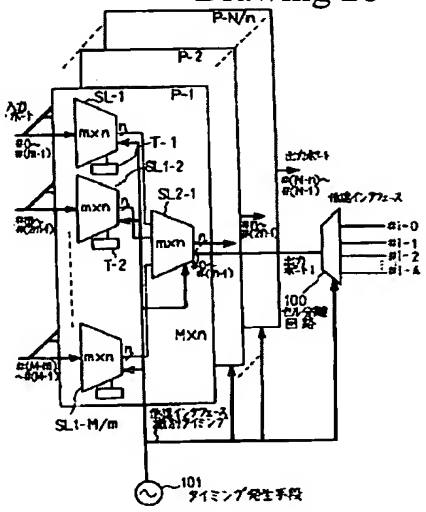


第2の単位スイッチ（低速インタフェース対応）

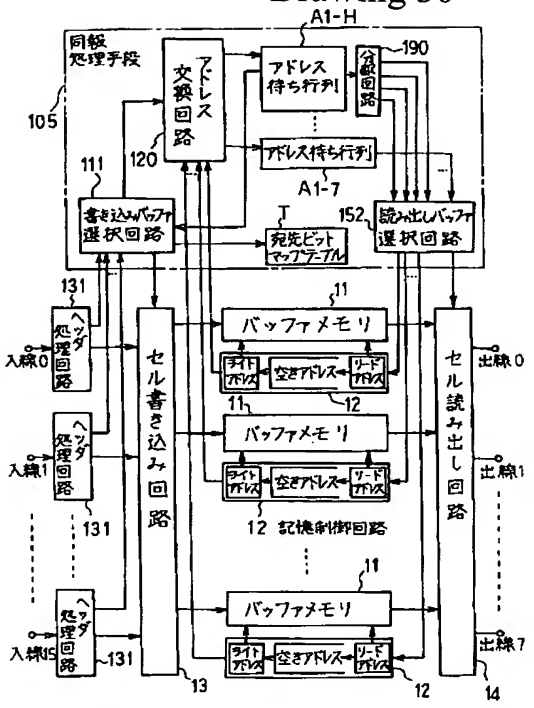
Drawing 46



Drawing 28

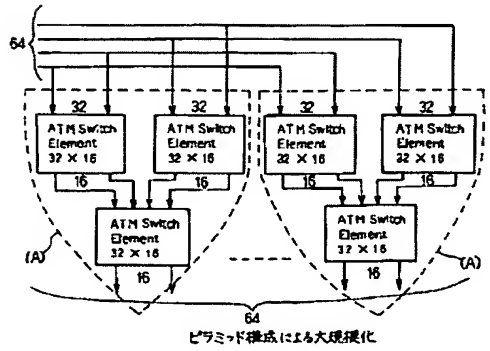


Drawing 30



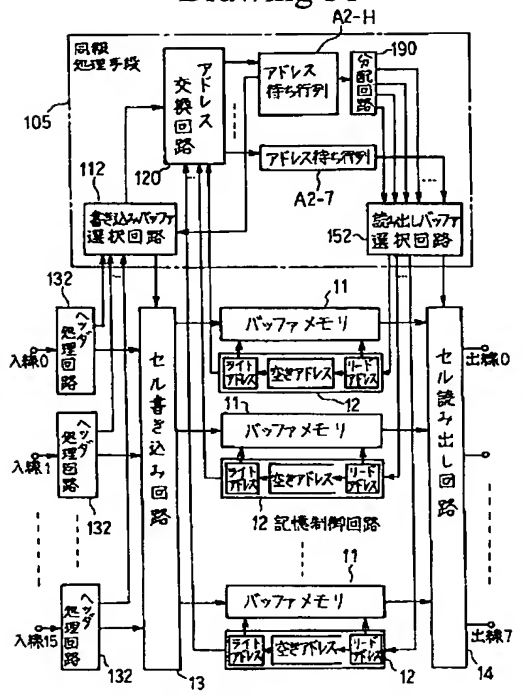
第1の単位スイッチ(高速インタフェース対応)のブロック図

Drawing 39



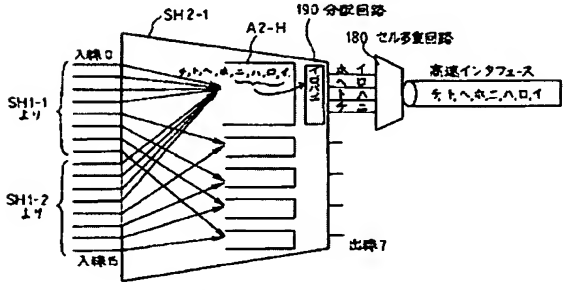
ピラミッド構成による大規模化

Drawing 31



第2の単位スイッチ（高速インタフェース対応）のブロック図

Drawing 33



第2の単位スイッチの動作例

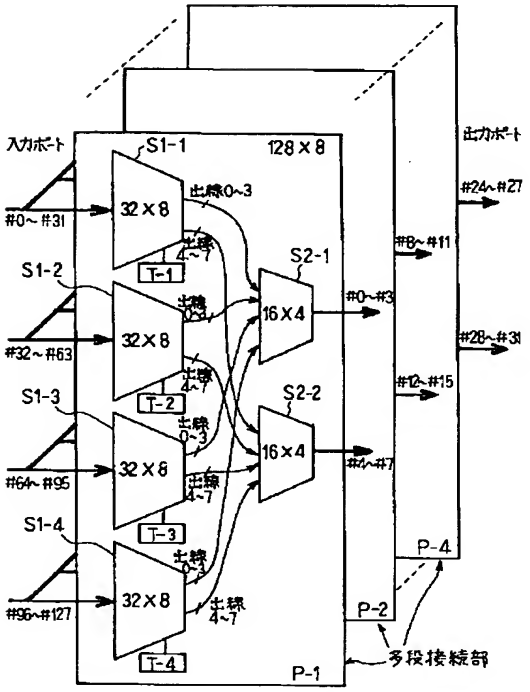
Drawing 37

方式	全てビットマップ表現	同報のみビットマップ表現
テーブル容量	32×3+16=112bit 112bit×64Kw=7168Kbit	5×3+16+1=32bit 32bit×64Kw=2048Kbit 32bit×4K×3/32=12Kbit Total 2060Kbit
容量比	3．5	1

ＶＣＩ　　：１６ビット
入線／出線数：32

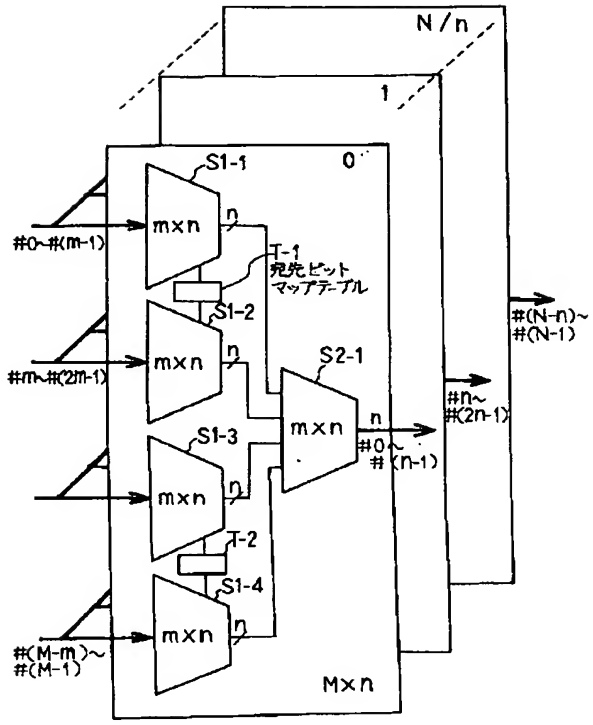
ルート情報テーブル容量比較

Drawing 34



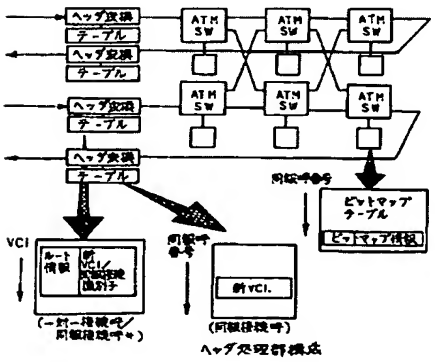
2段接続による128×32スイッチの構成図
第1の単位スイッチ（32×8），第2の単位スイッチ（16×4）

Drawing 35

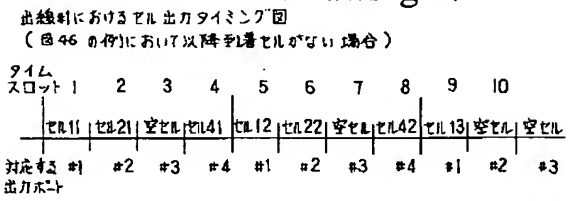


宛先ビットマップテーブルを共有化する場合

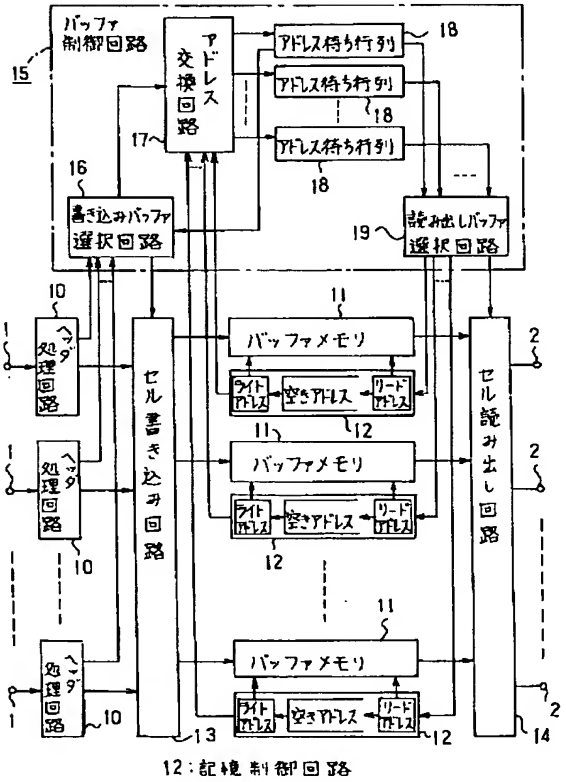
Drawing 38



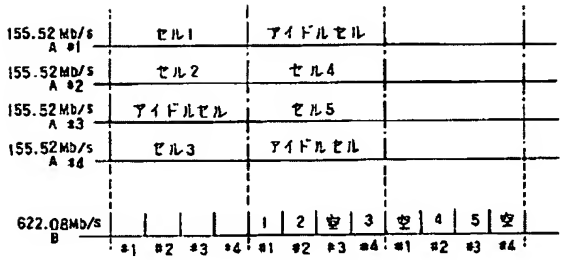
Drawing 47



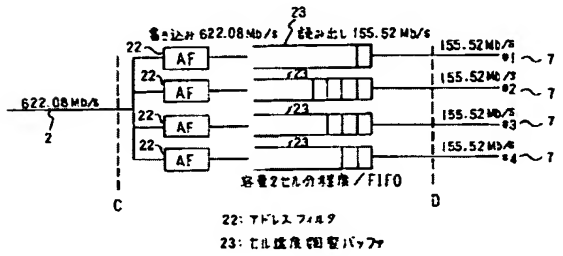
Drawing 41



Drawing 43



Drawing 44



Drawing 45